工業技術研究院
Industrial Technology
Research Institute

ESL Trends and Opportunities

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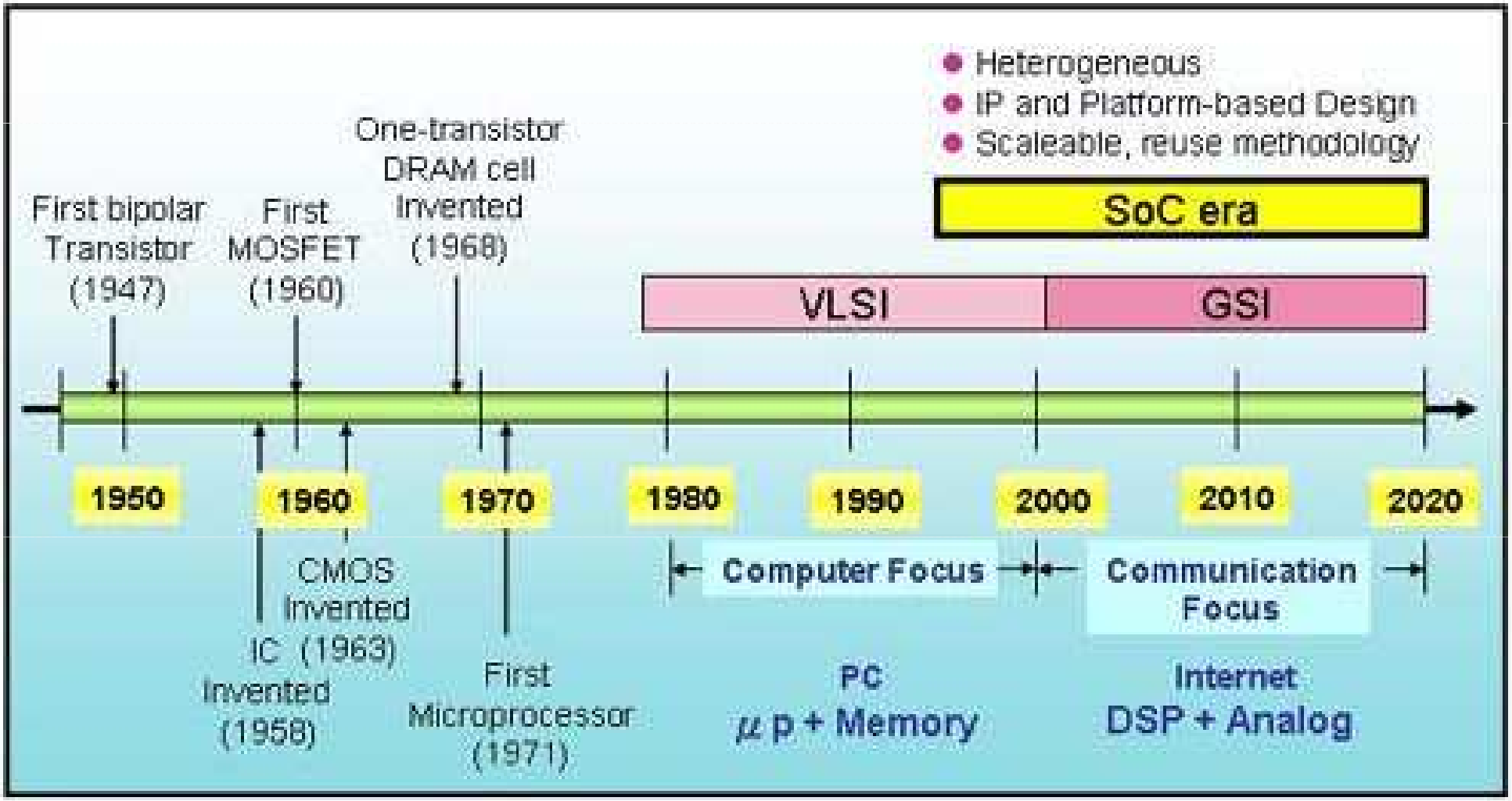
2009/10/02

Agenda

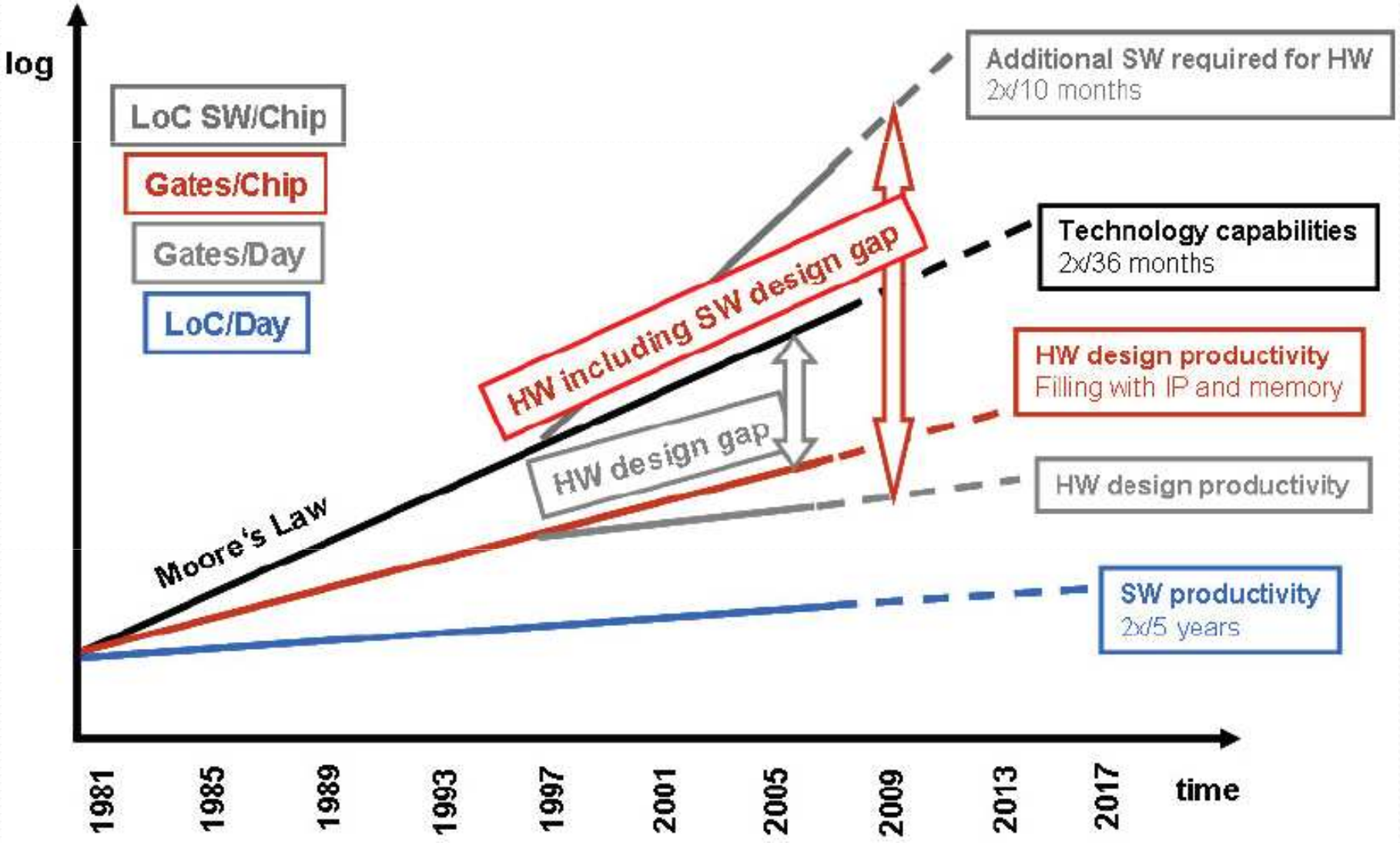
- Introduction to ESL
- OSCI SystemC
- Transaction Level Modeling
- DAC 2009 Highlights
  - Trends and Opportunities
- Summary

Evolution of Silicon Technology



Source: MIRC, NCTU

HW & SW Productivity Gap



Source: ITRS, 2007

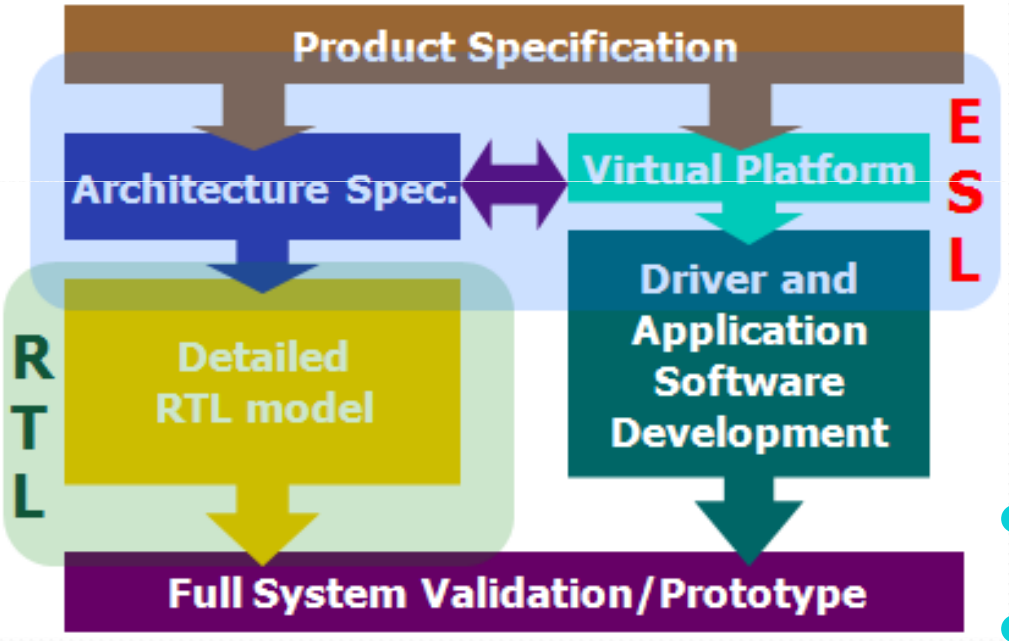
Silicon Design Methodologies

- In Silicon Design we have progressed through three major design methodologies and are heading into a fourth.
  - 1964 Transistor Level Design (IC CAD)
  - 1980 Gate Level Design (IC CAE)
  - 1987 Register Transfer Level Design (RTL)
  - 2005 Electronic System Level Design (ESL)

ESL Definition ---wikipedia

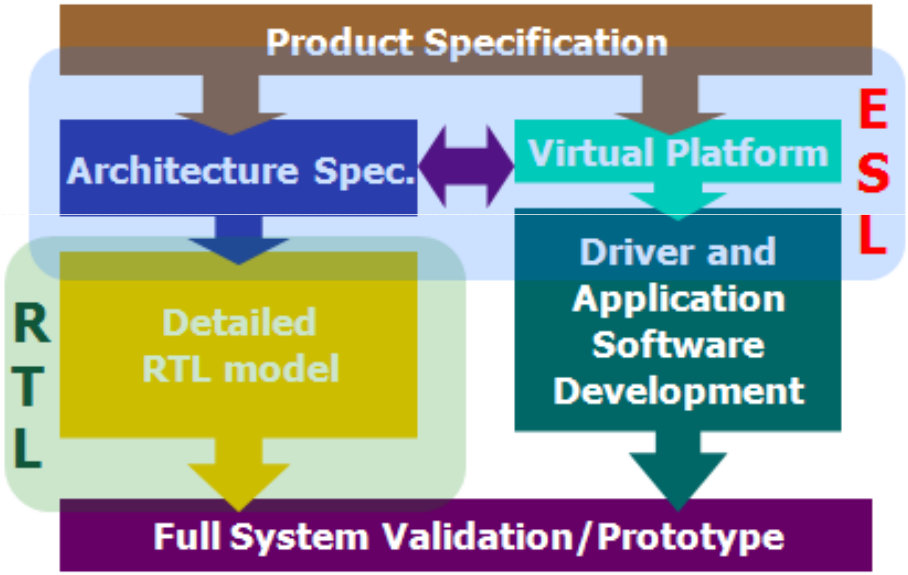
- Electronic System Level
  - An emerging electronic design methodology that focuses on the higher abstraction level concerns first and foremost

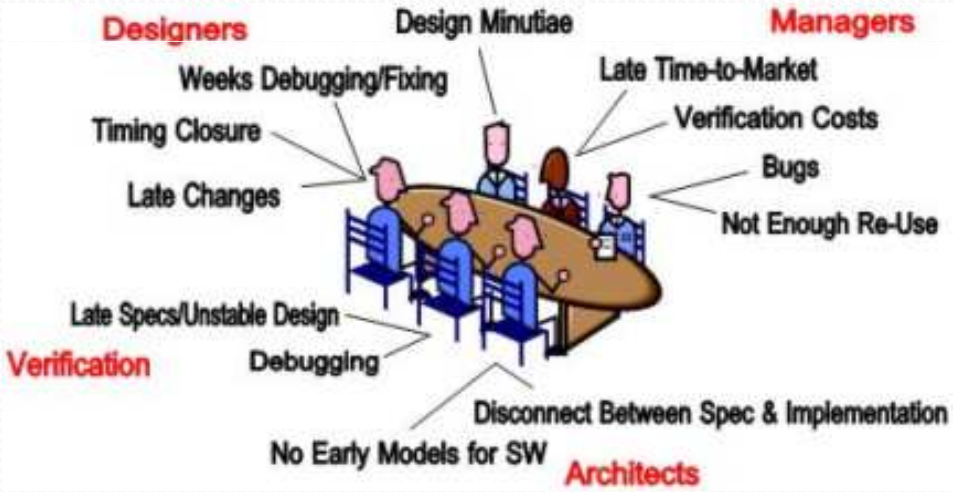
ESL Advantages



- System-level design
- HW/SW co-design
- Architecture exploration
- Virtual prototyping
- Co-simulation/co-verification

ESL Advantages (Verification)

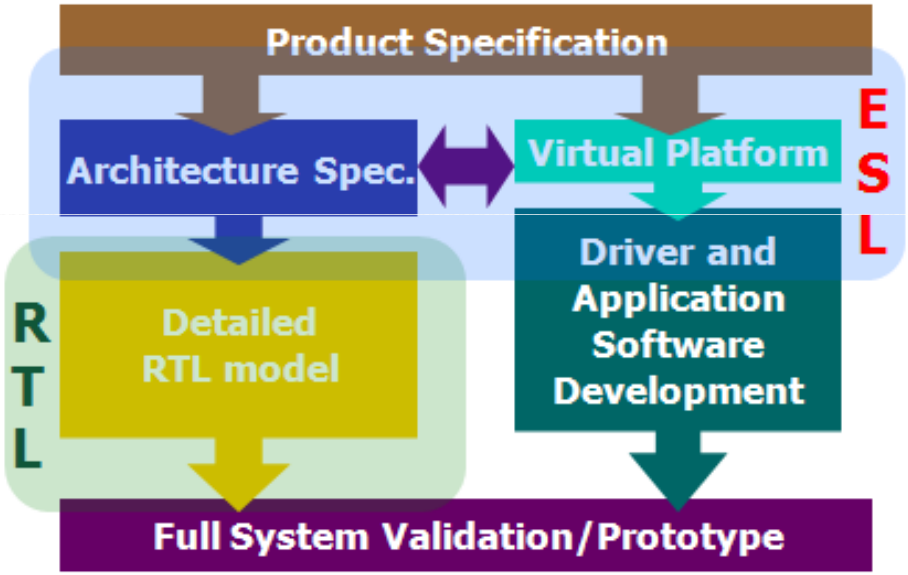


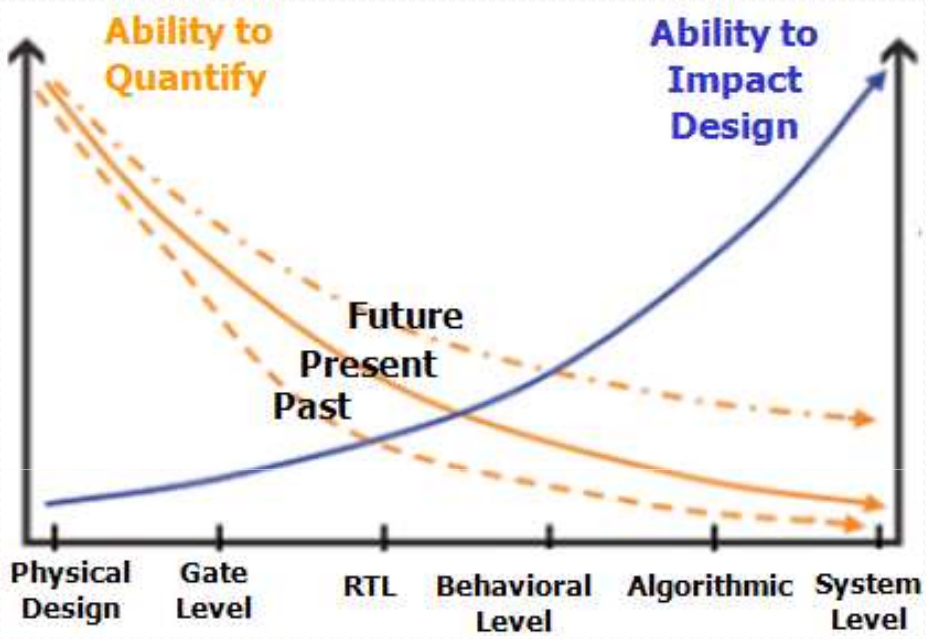


Unified design and verification environment, that all the development parties can use

Source: ARM, Intel, Chip Design Magazine

ESL Advantages (Exploration)

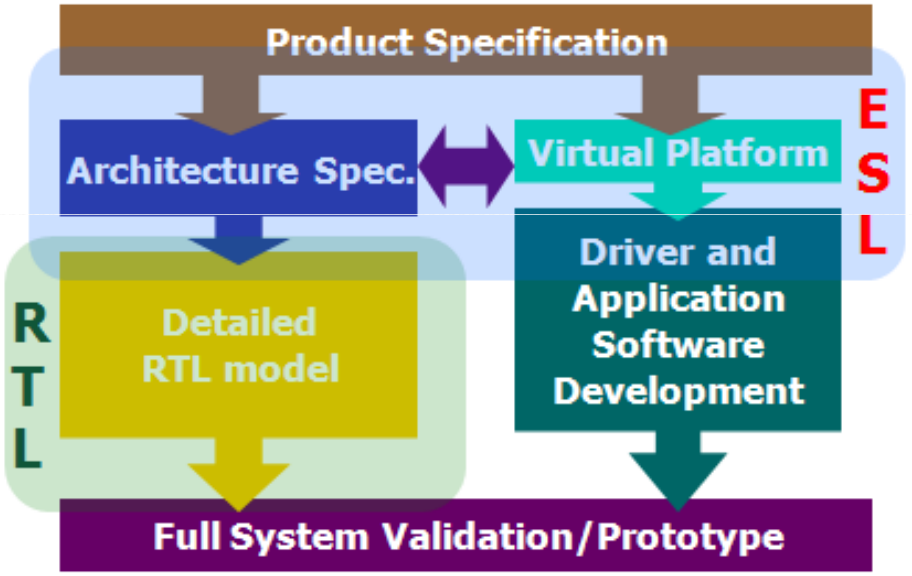


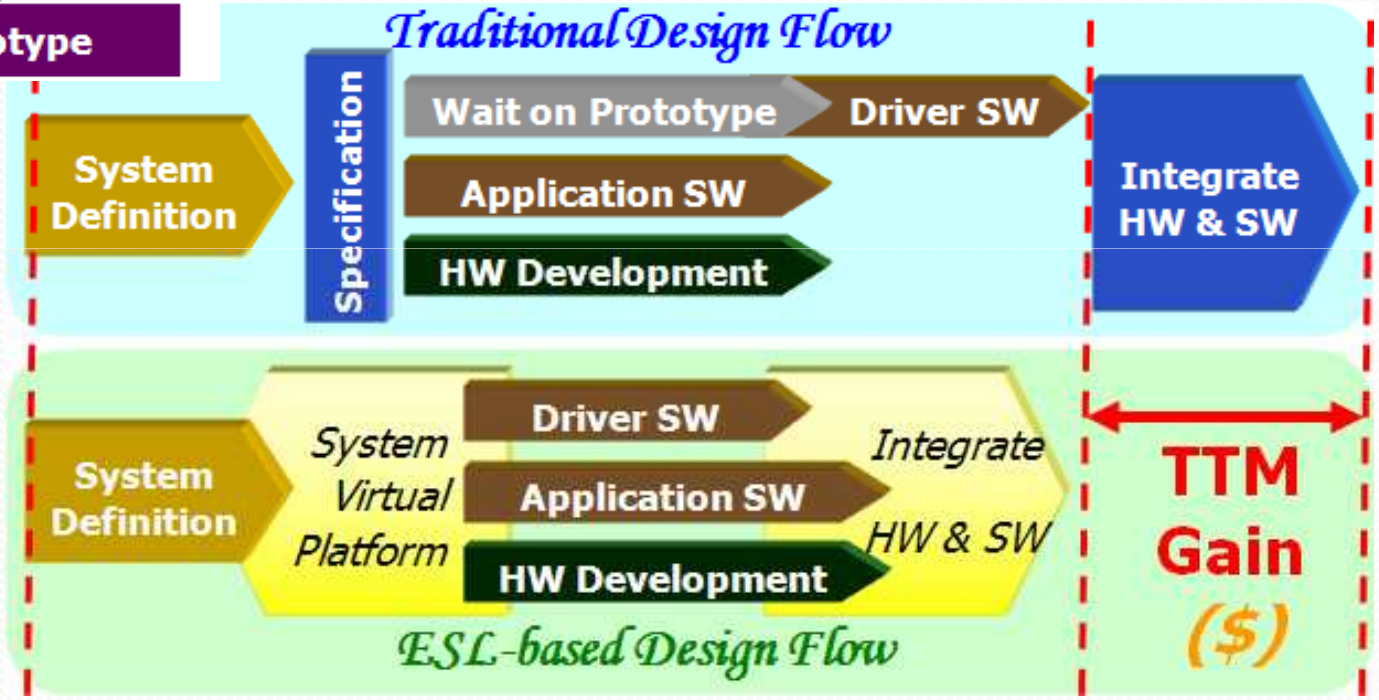


System architecture exploration and power estimation

Source: ARM, Intel, Chip Design Magazine

ESL Advantages (TTM)





Source: ARM, Intel, Chip Design Magazine

SystemC Overview

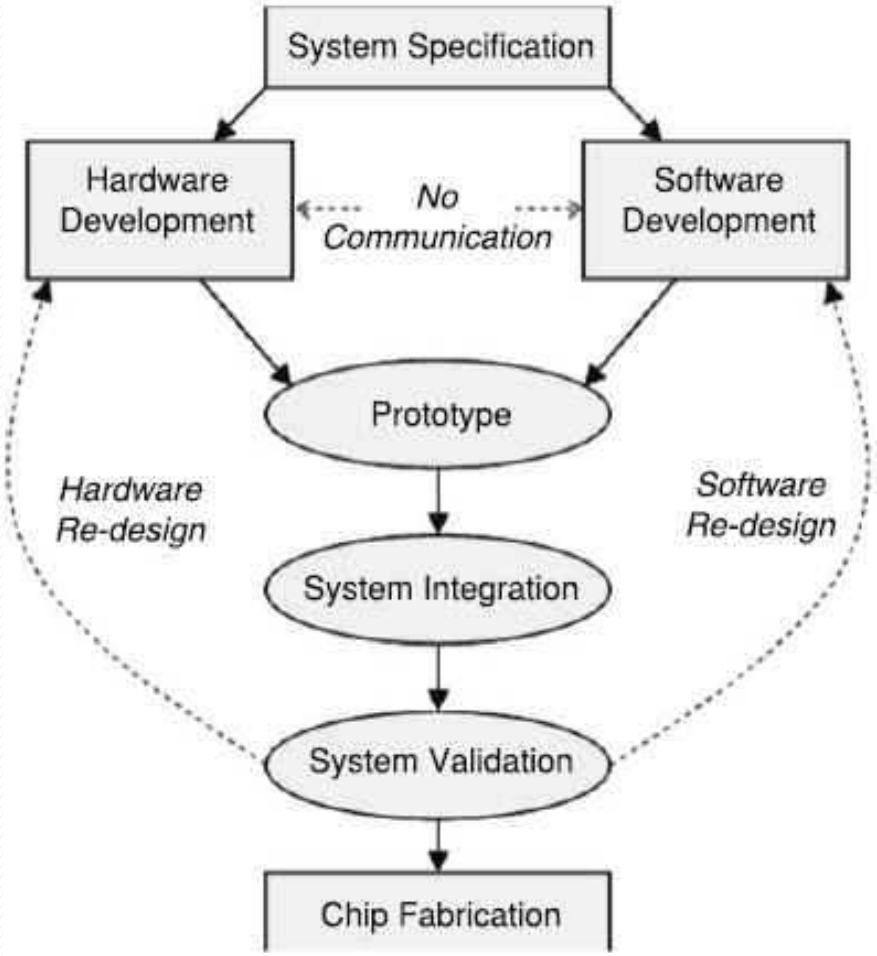
- Is an HDL, not designed for implementing SW, although it was the original intention in making it a language that can describe both
  - Version 1: just another HDL, not much to do with system-level designing
  - Version 2: became a system-level language with the adding of channel
  - Version 2.1: adding some programming language features and simulation semantics.
  - IEEE approved OSCI* SystemC 2.1 as the IEEE 1666 Standard on 12/12/2005

* OSCI: Open SystemC Initiative

SystemVerilog vs. SystemC

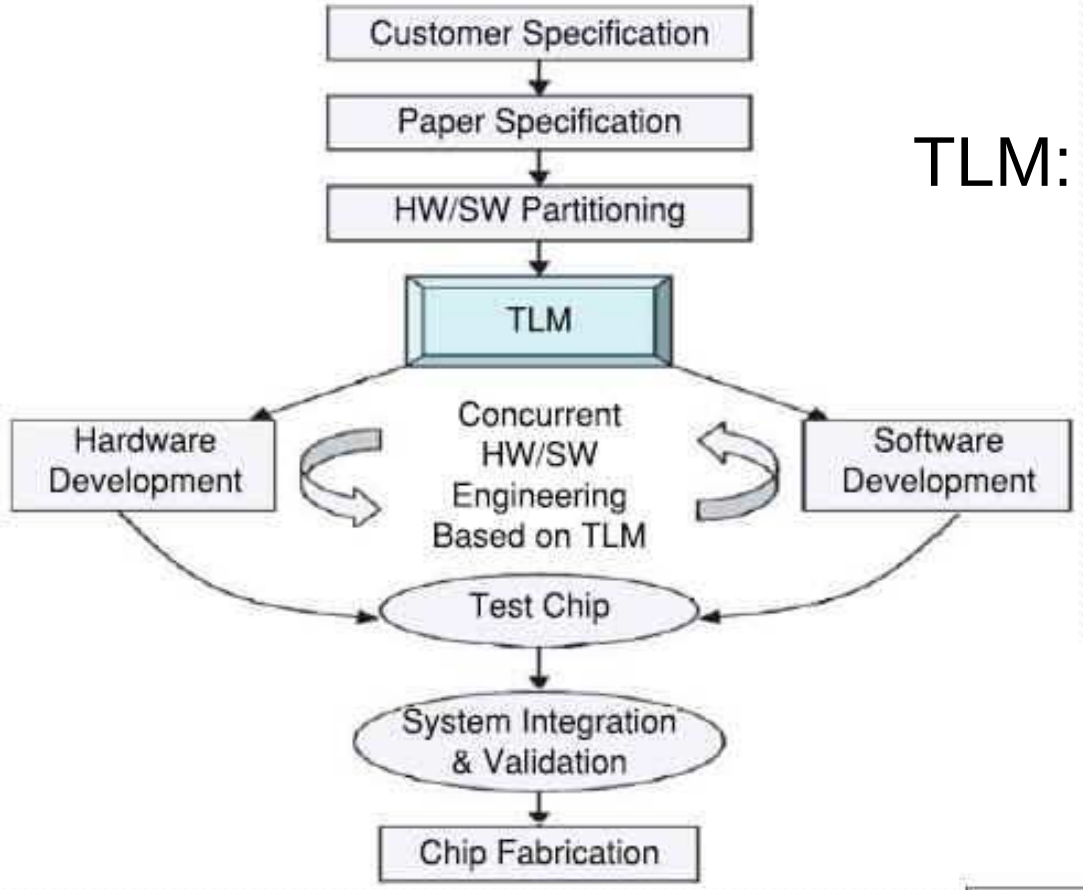
- IEEE approved Accellera SystemVerilog 3.1a as IEEE 1800 Standard on 11/8/2005
- SystemVerilog is Verilog plus verification (assertion)
- Actually the above statement is not fair but it is the truth now
- SystemVerilog and SystemC work together to complete the design platform from system-level to gate-level
- SystemC deals with whatever above RTL
- SystemVerilog deals with RTL and below

Classic Design Flow

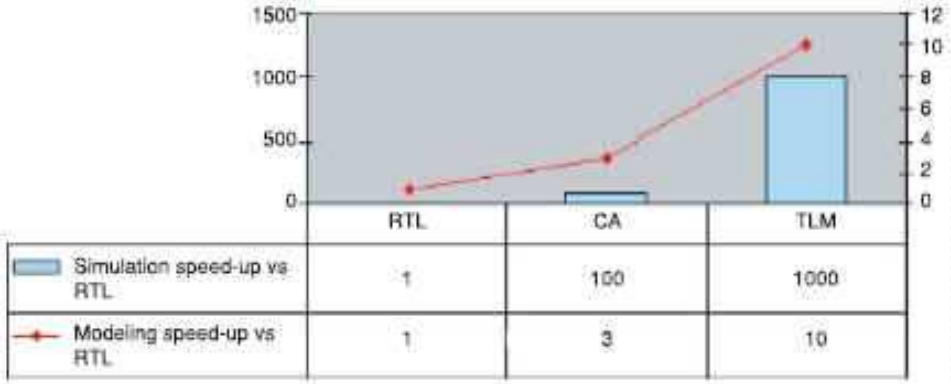


Source: “Transaction-Level Modeling with SystemC: TLM Concepts and Applications for Embedded Systems”, Springer, 2005

Novel SoC Design Flow

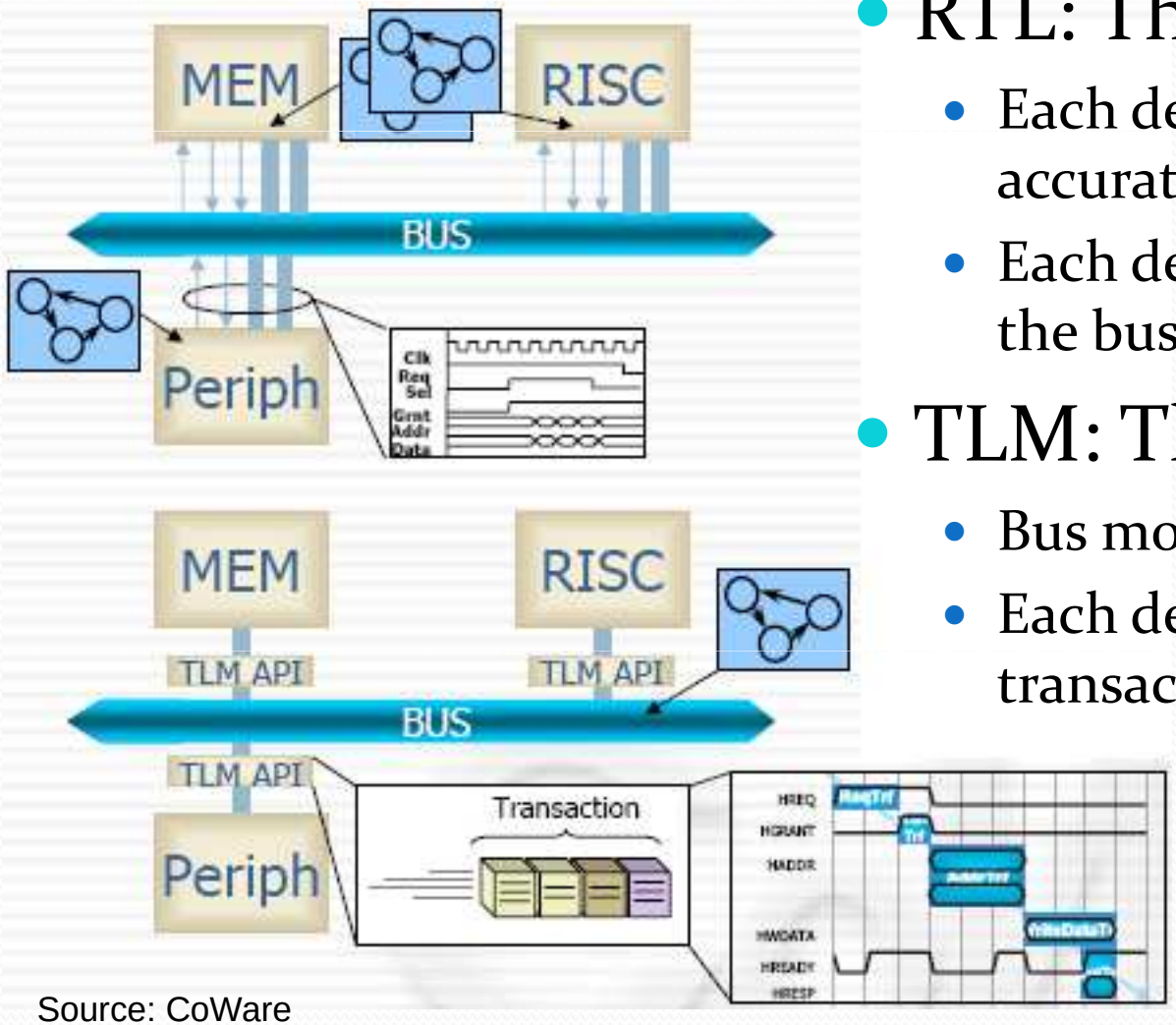


TLM: Transaction Level Modeling



Source: “Transaction-Level Modeling with SystemC: TLM Concepts and Applications for Embedded Systems”, Springer, 2005

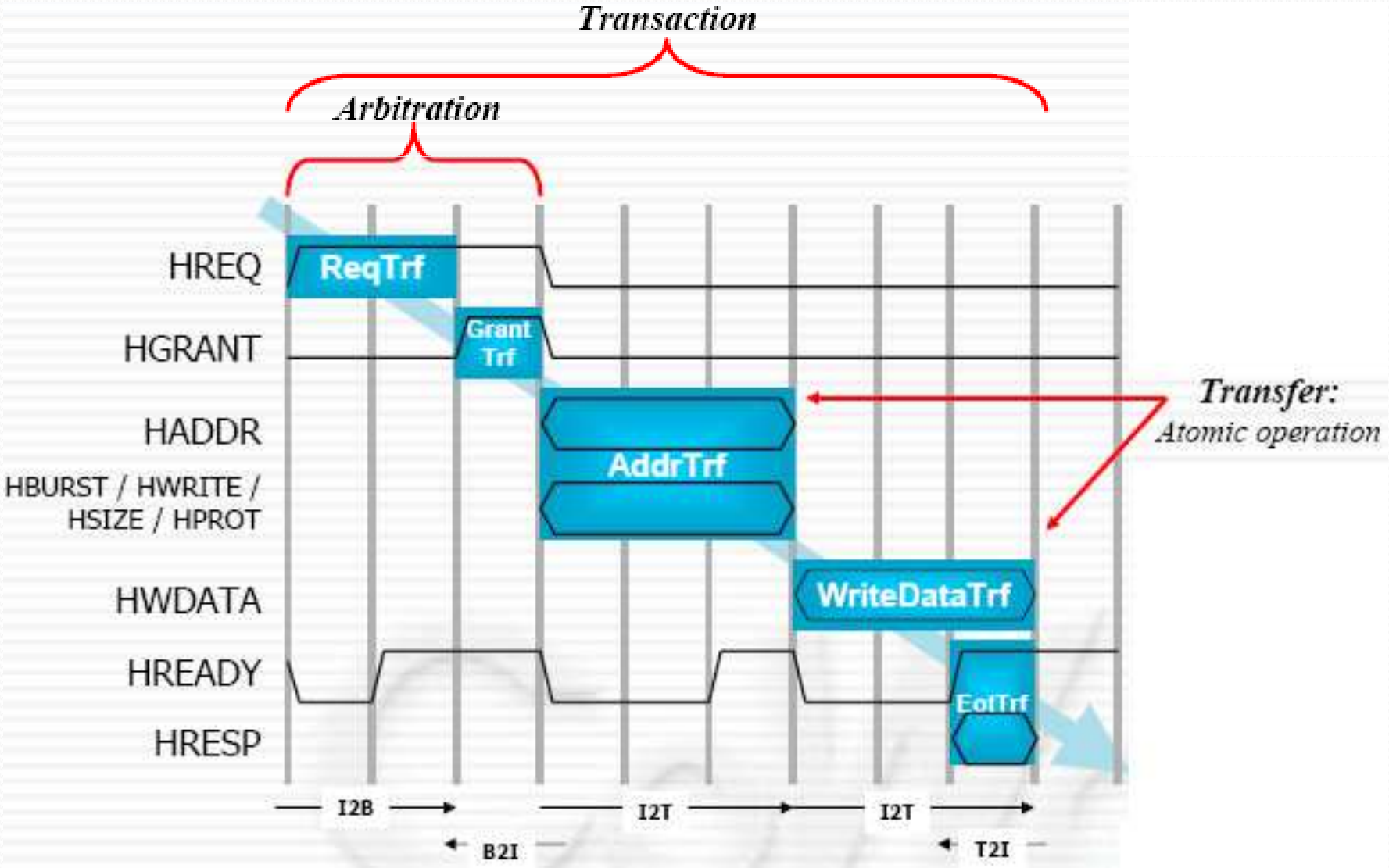
A Higher Level of Abstraction



Source: CoWare

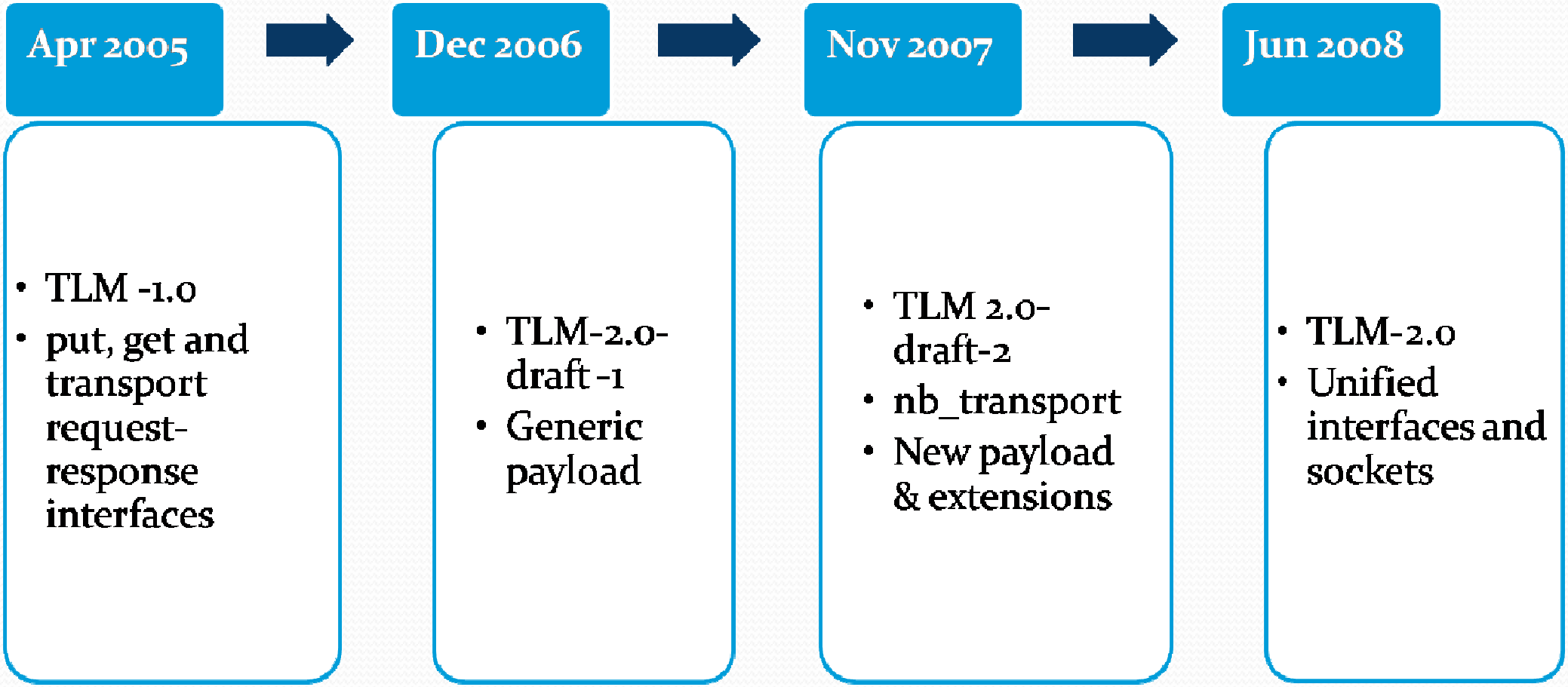
- RTL: The bus is merely wires
  - Each device on the bus has a pin-accurate interface
  - Each device interface must implement the bus protocol
- TLM: The bus model is key
  - Bus model enforces the bus protocol
  - Each device communicates via transaction level API

Transaction & Transfer



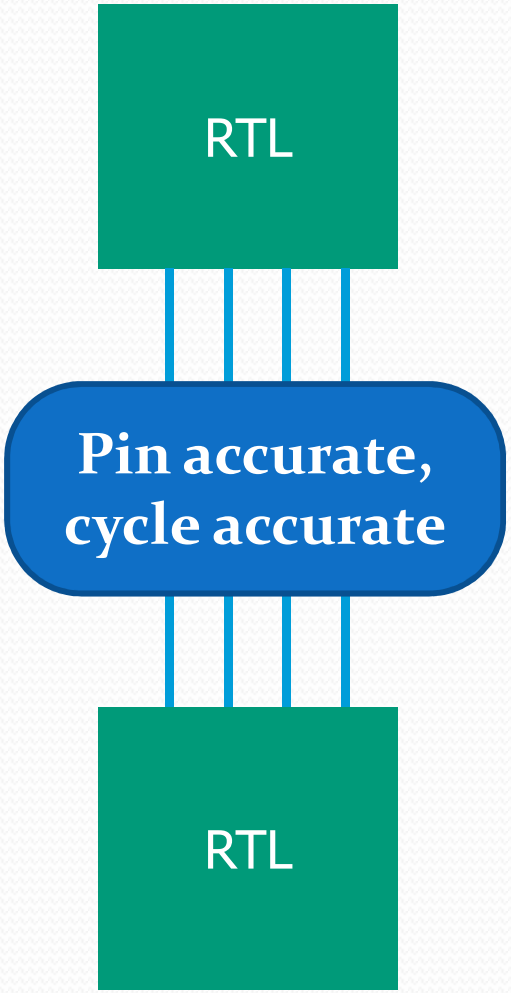
Source: CoWare

OSCI TLM Development

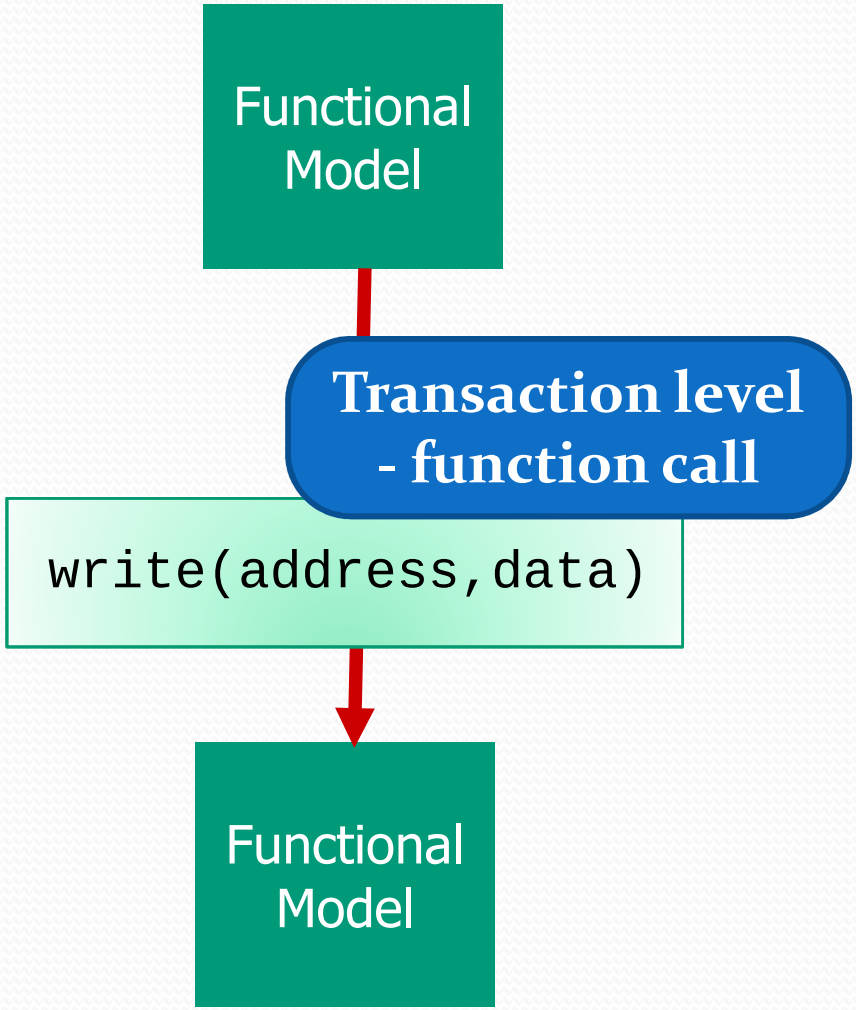


Source: OSCI

RTL vs. TLM



Simulate every event



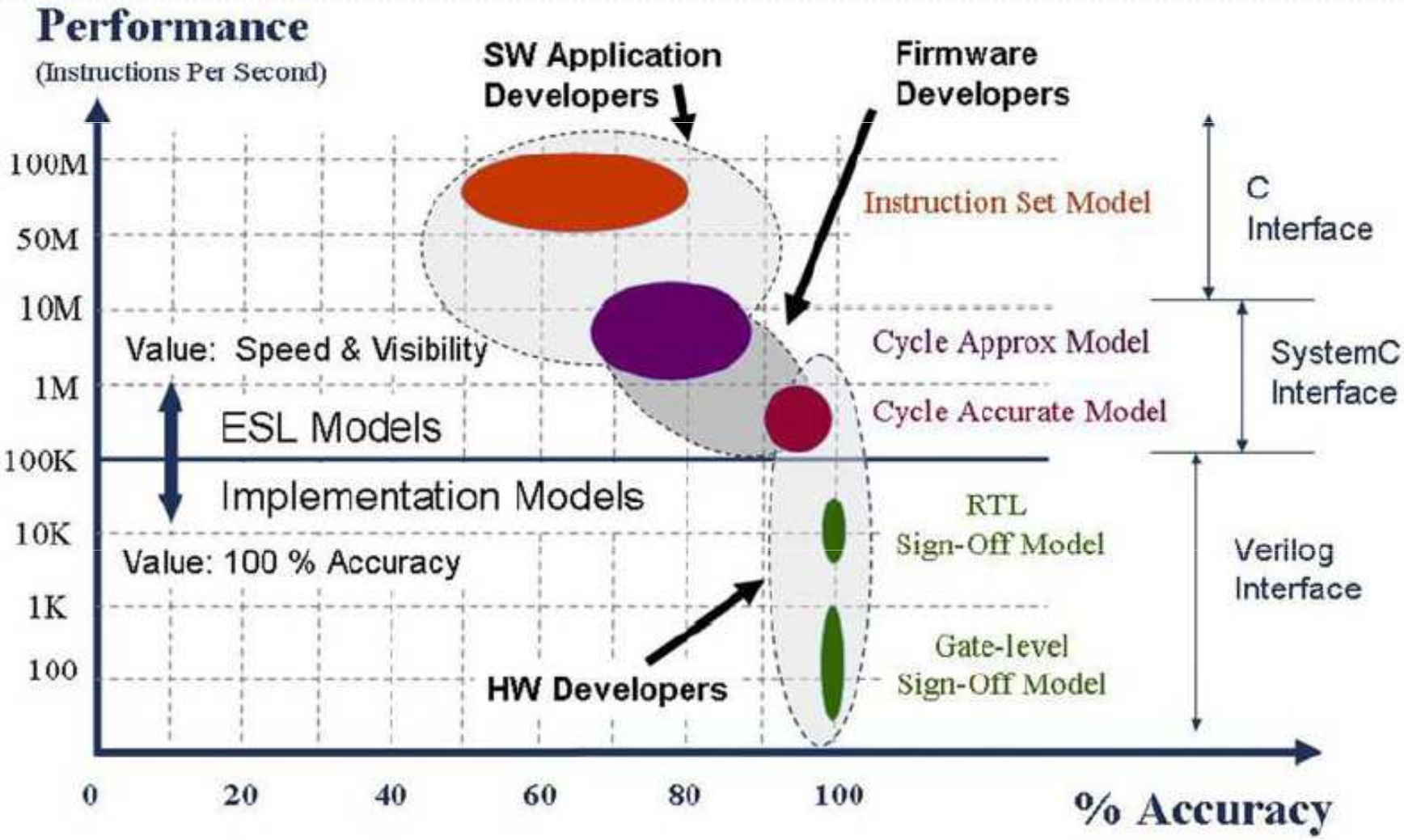
100-10,000 X faster simulation

Source: OSCI

Transaction Level Modeling

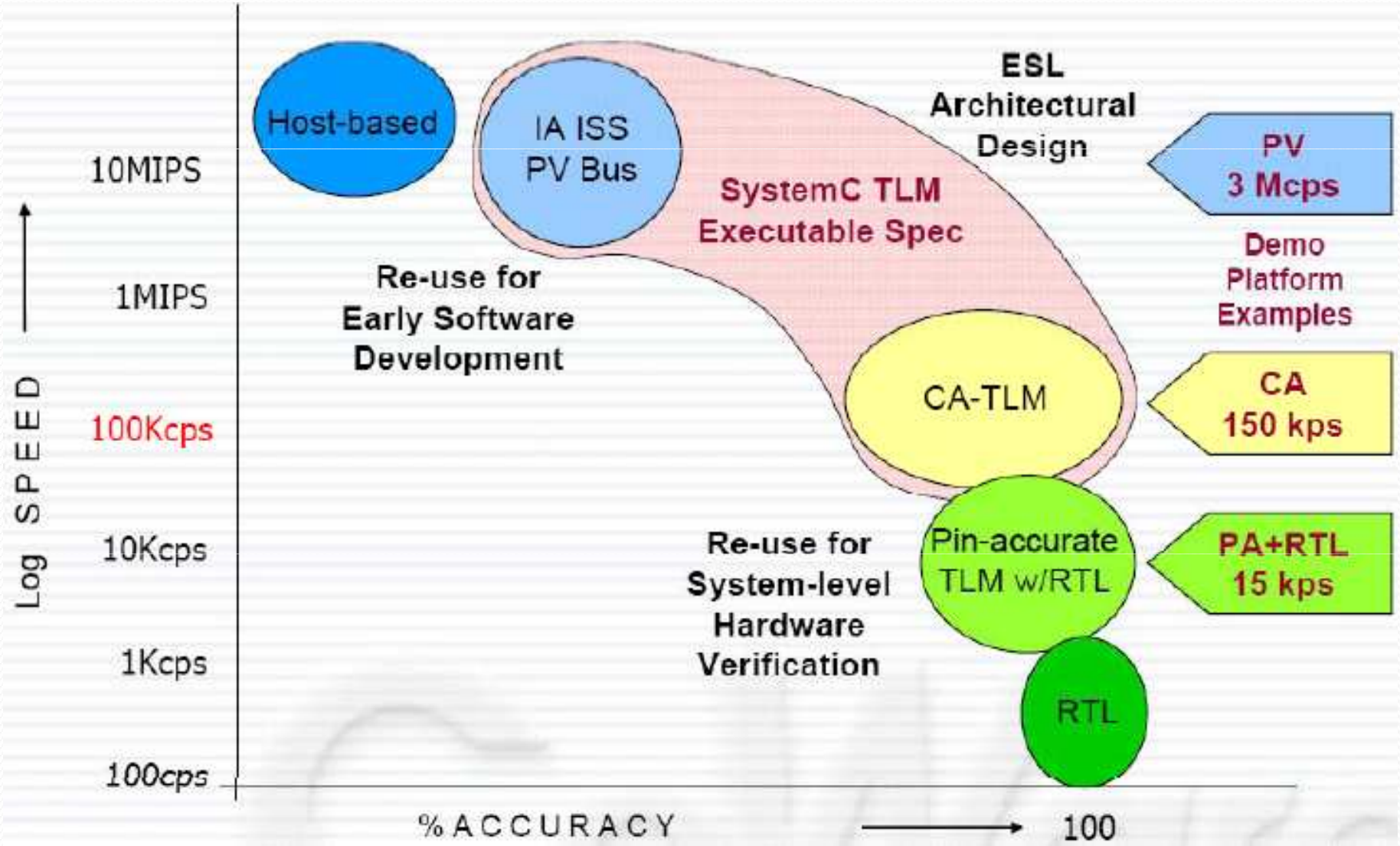
- The TLM serves as the unique reference across different teams
  - Software team
    - The TLM serves as the reference for earlier software development
  - Hardware team
    - The TLM serves as the reference for coarse-grain architecture analysis
  - Verification team
    - The TLM serves as the golden model to generate functional verification tests that will be applied on the RTL platform once it become available

Abstraction Level



Source: ARM white paper---Taking Design to the System Level

Simulation Speed vs. Accuracy



Source: CoWare

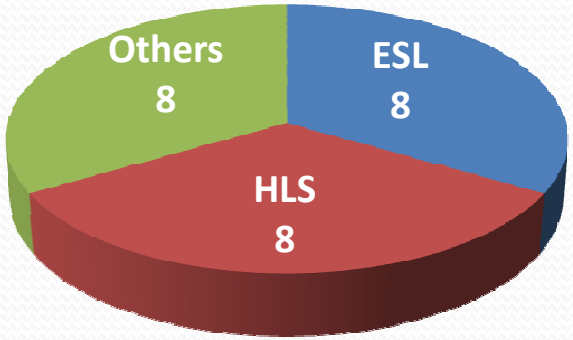
DAC 2009 Highlights Trends and Opportunities

DAC 2009 Highlights

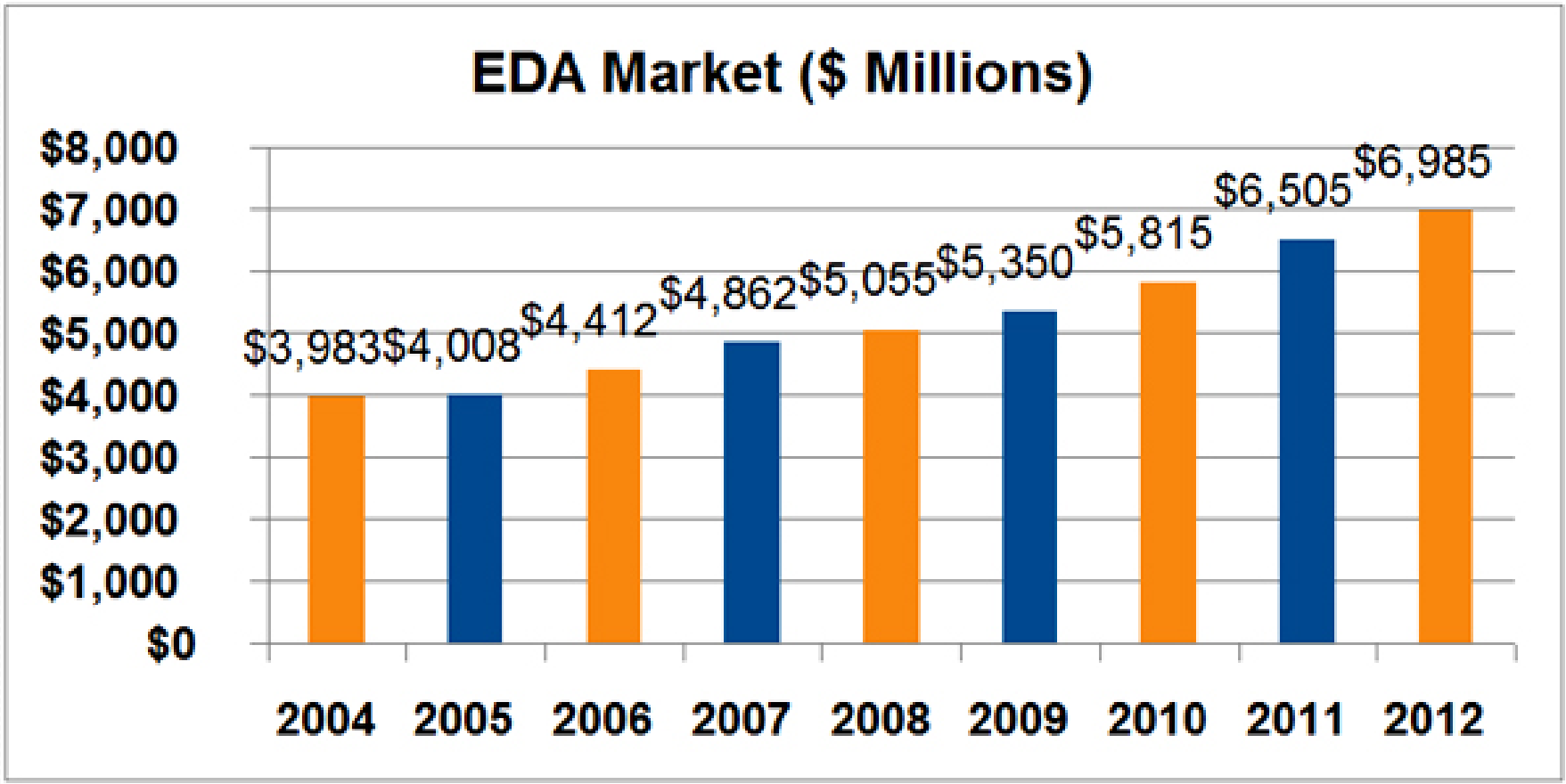
- Design Automation Conference
  July 25-30, San Francisco, CA
- 7,996+ attendees
- Selected 148 papers from 684 submissions
- 29 first-time participating companies from 202 companies (~14%)
- Additional events:
  - 8 workshops, 11 collocated events, 6 tutorials, 10 user tracks

Gary Smith's Talk

- EDA Trends and What's Hot at DAC
- *"I Love DAC"* at the beginning
- Emphasized "ESL, ESL, and ESL"
- *"What To See"* list
  - Total companies: 24
  - ESL-related: 16
  - High-level synthesis: 8



EDA Industry Revenues



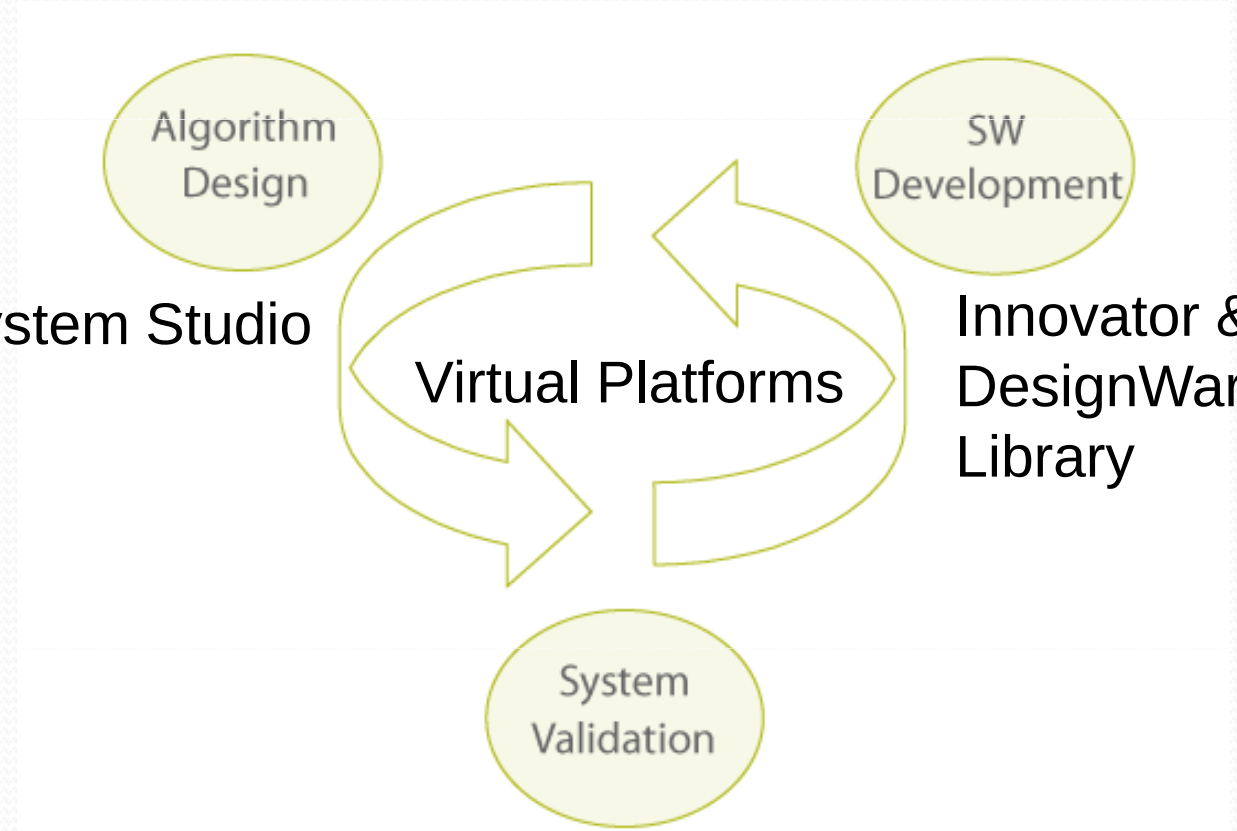
Source: Gary Smith EDA, 2008

Keynote Address

- Presenter: TSMC VP Fu-Chieh Hsu
- Title: ” Overcoming the New Design Complexity Barrier: Alignment of Technology and Business Models”
- Open Innovation Platform (OIP)

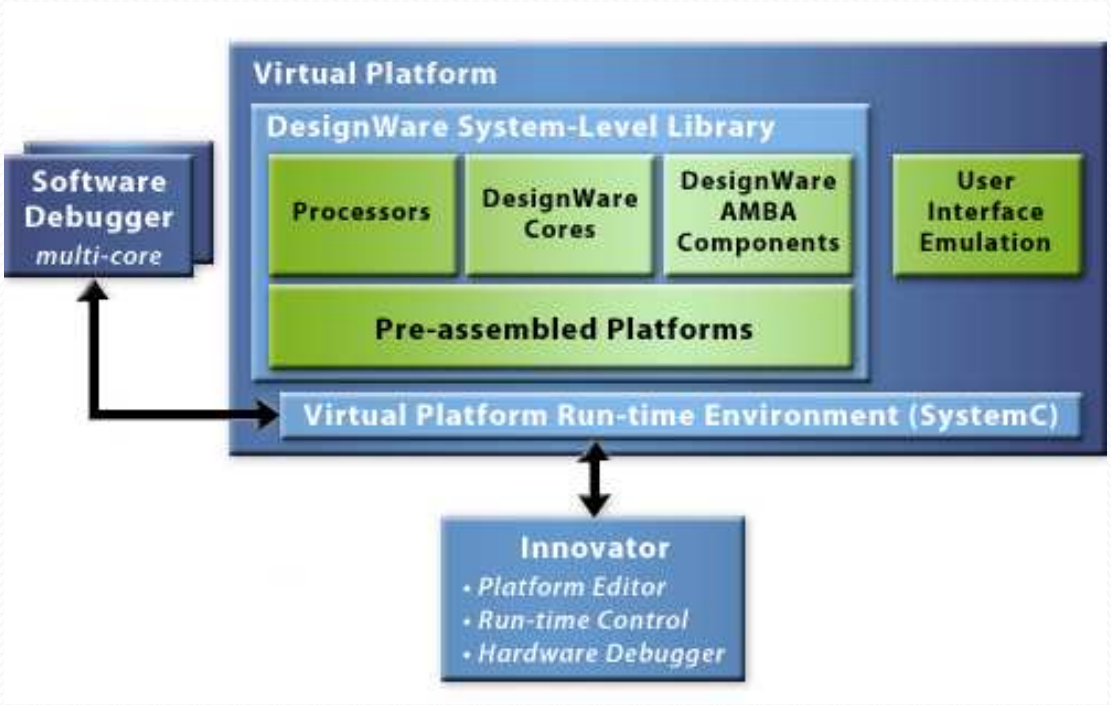
EDA Companies Exhibit

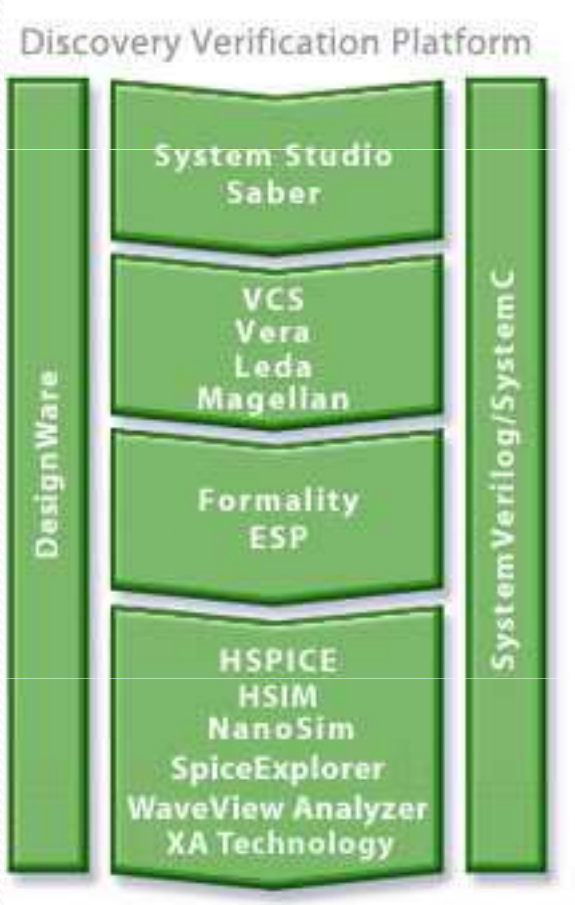
Synopsys System-Level Solutions



Source: Synopsys

Synopsys Virtual Platform and Verification Platform





Source: Synopsys

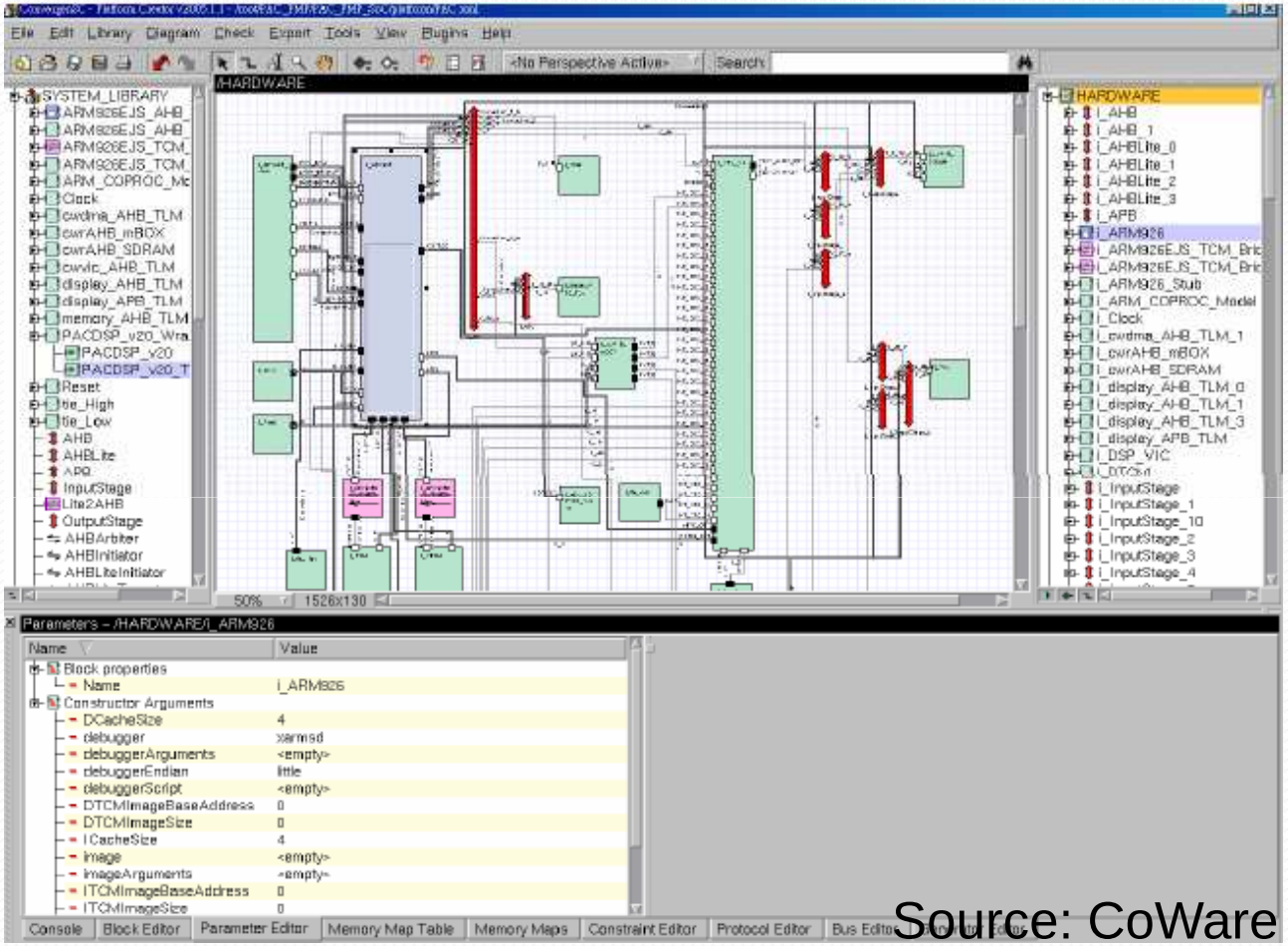
Synopsys System-Level Services

- Model creation
- Virtual platform assembly/customization
- System-level methodology consulting

Vendor	Architecture	Virtual Platforms
ARM		VPAI
Freescale	i.MX31	VPMX31
Marvell	PXA	VPXA3
TI	OMAP, OMAPVox, Audio & Imaging Processors	VPOM serials, VPOM-V1030, VPDA295

CoWare

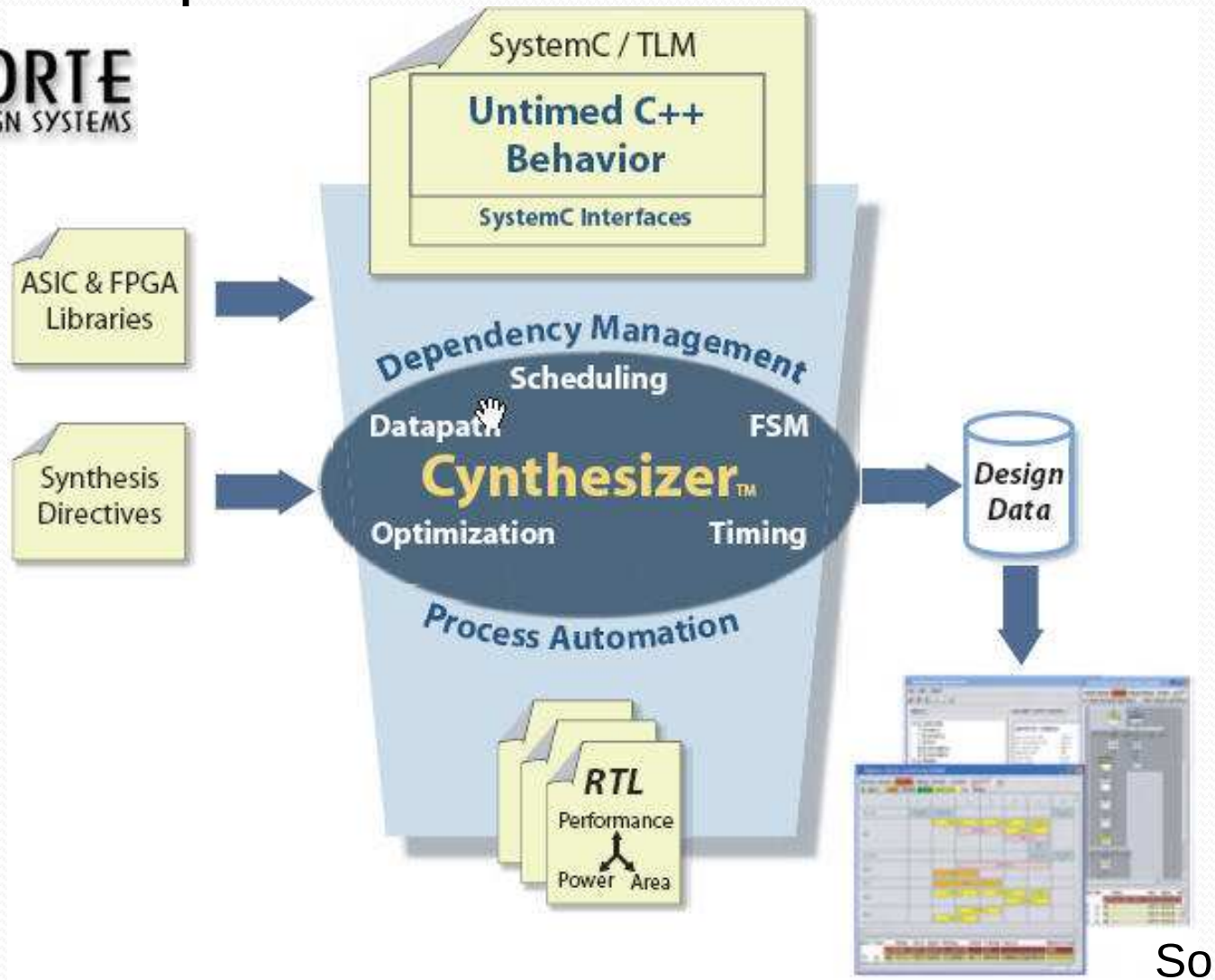
- Platform Architect
- Processor Designer
- Signal Processing Designer
- Virtual Platform
- Model Library
- ESL Consulting Services



Source: CoWare

FORTE Design Systems: Cynthesizer

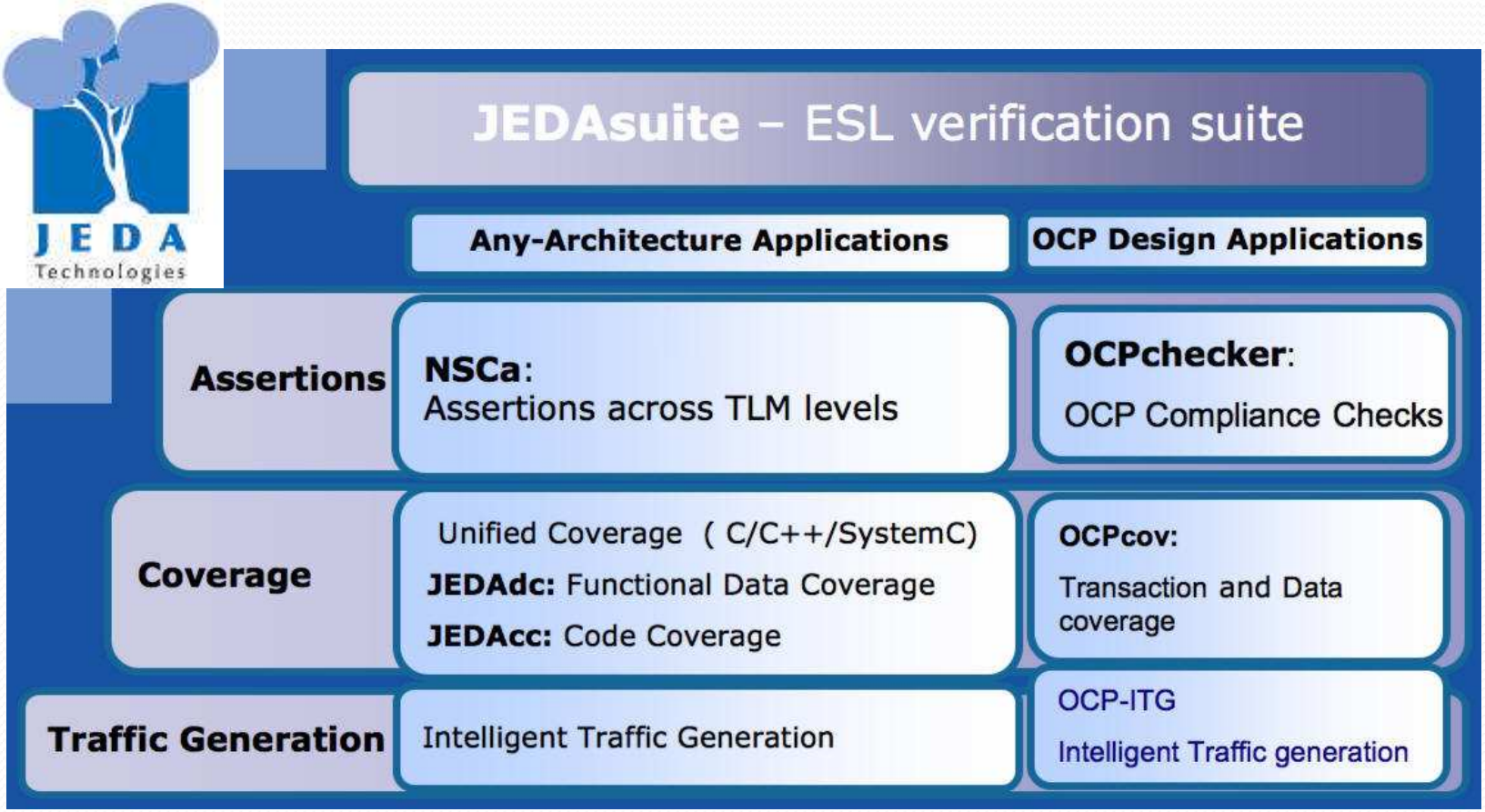
- TLM synthesis provider



Source: Forte

JEDA Technologies

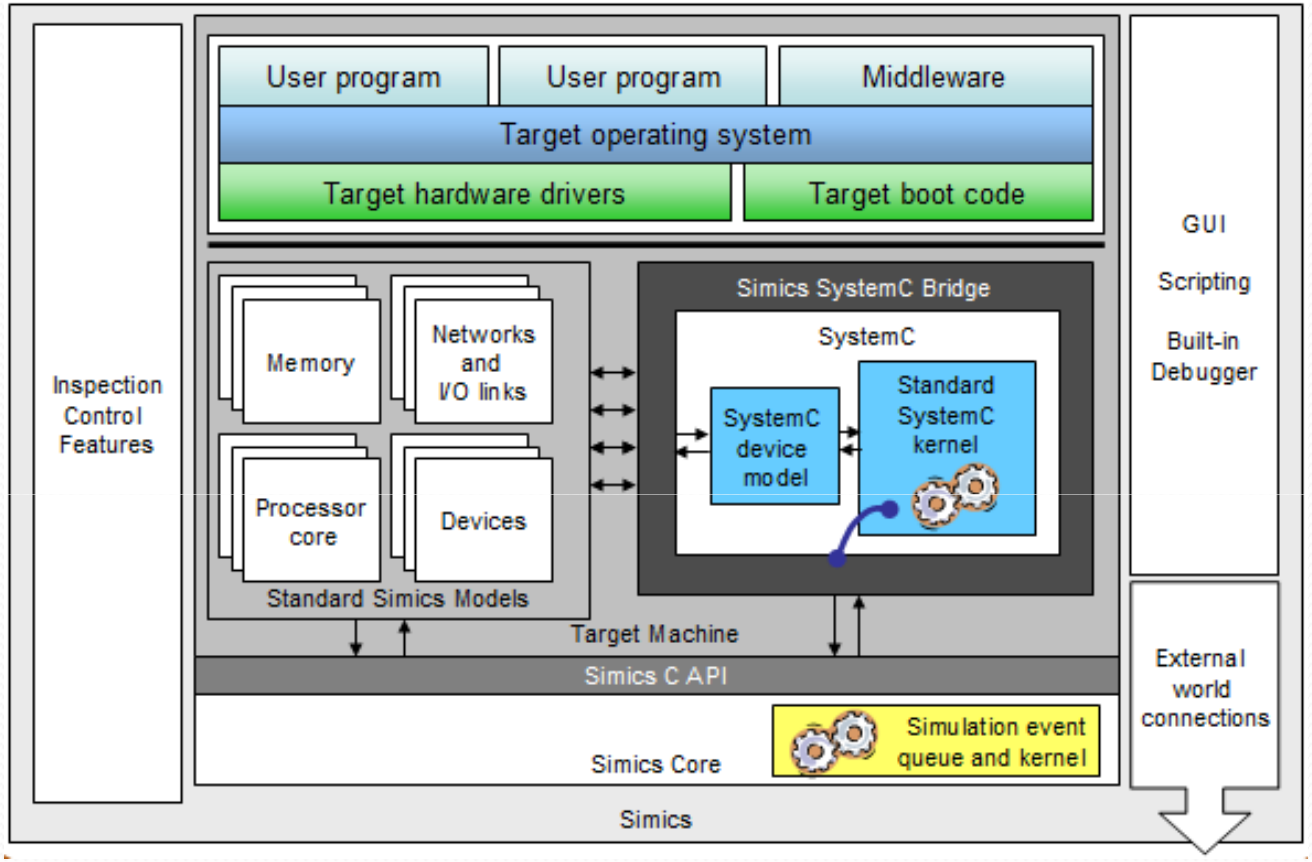
- ESL verification automation solutions



Source: JEDA

Virtutech: SIMICS

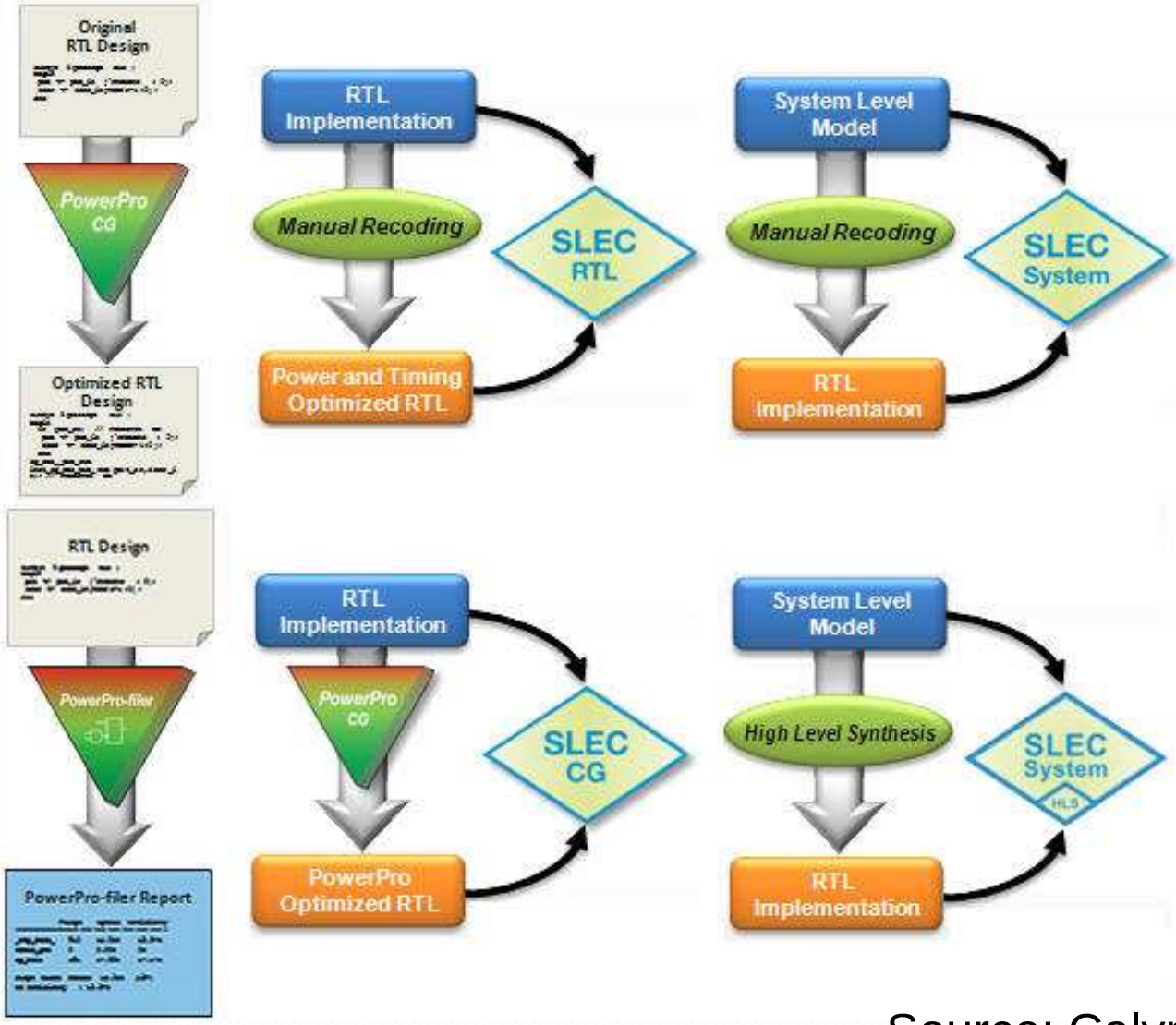
- A flexible and scalable software solution provider



Source: SIMICS

CALYPTO

- Power optimization and functional verification solutions provider

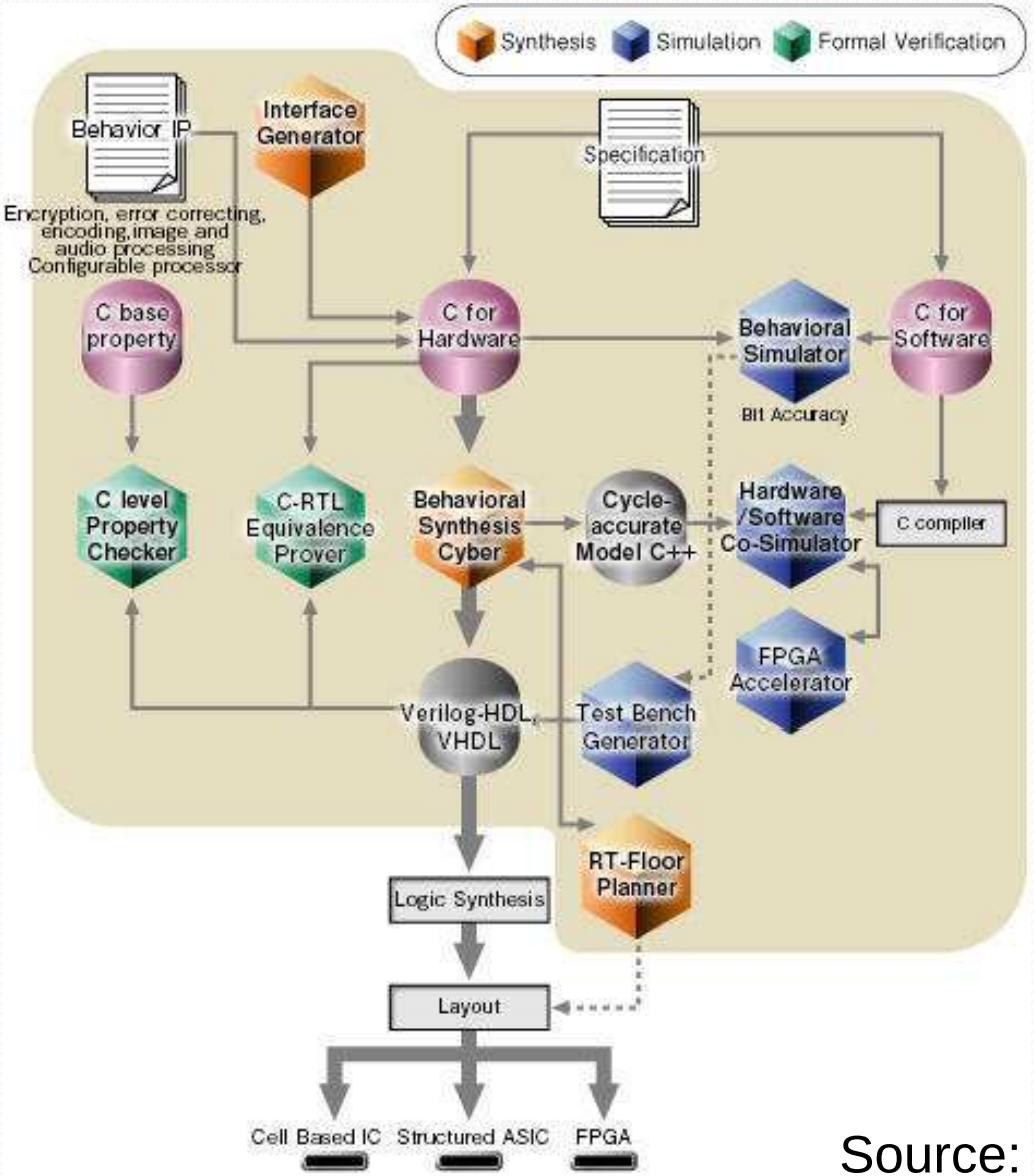


Source: Calypto

NEC CyberWorkBench

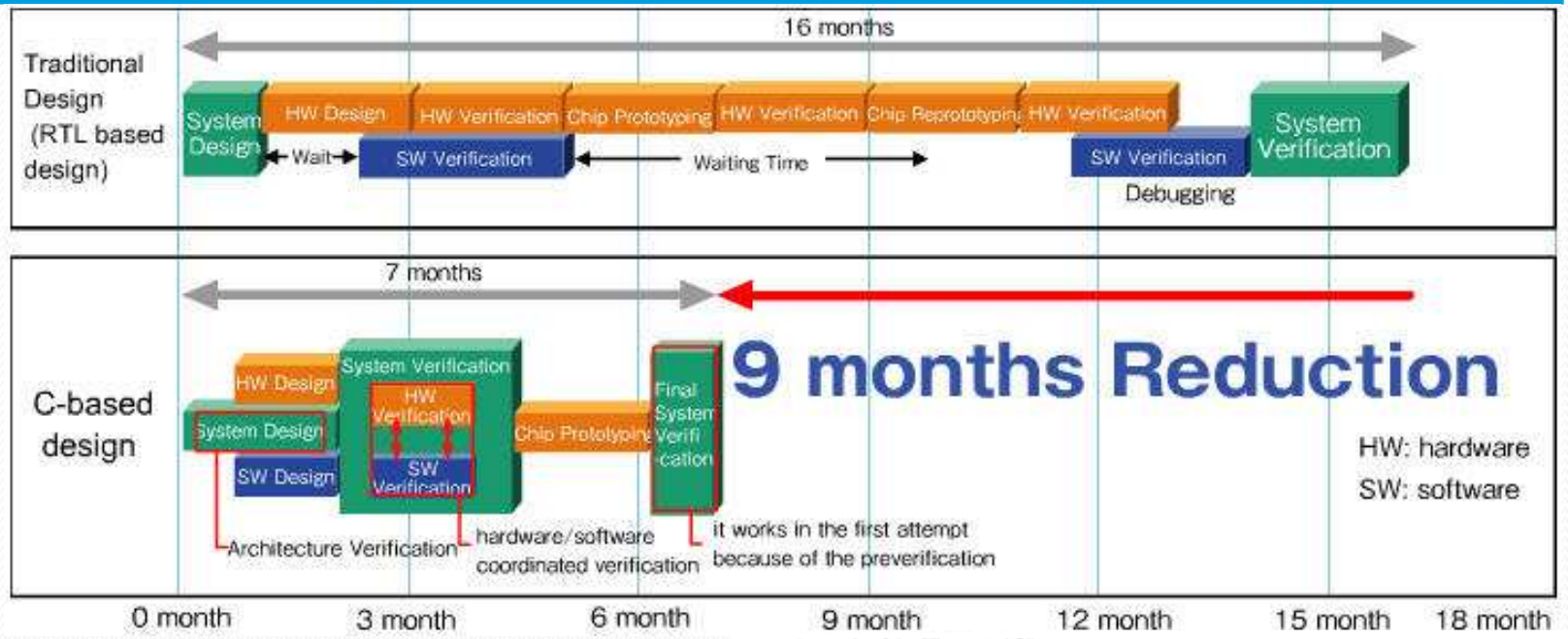
- C-based synthesis and verification environment for system LSI

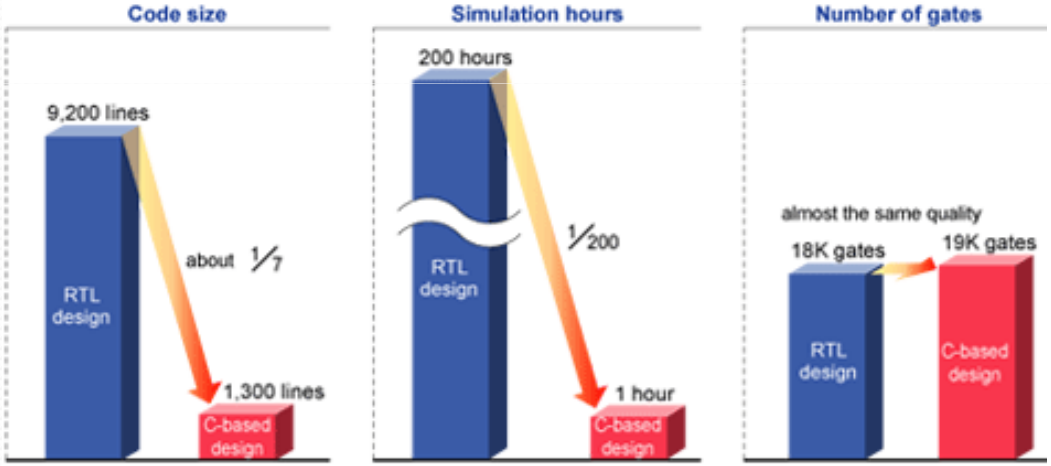
CyberWorkBench®
Pioneering C-based LSI Design

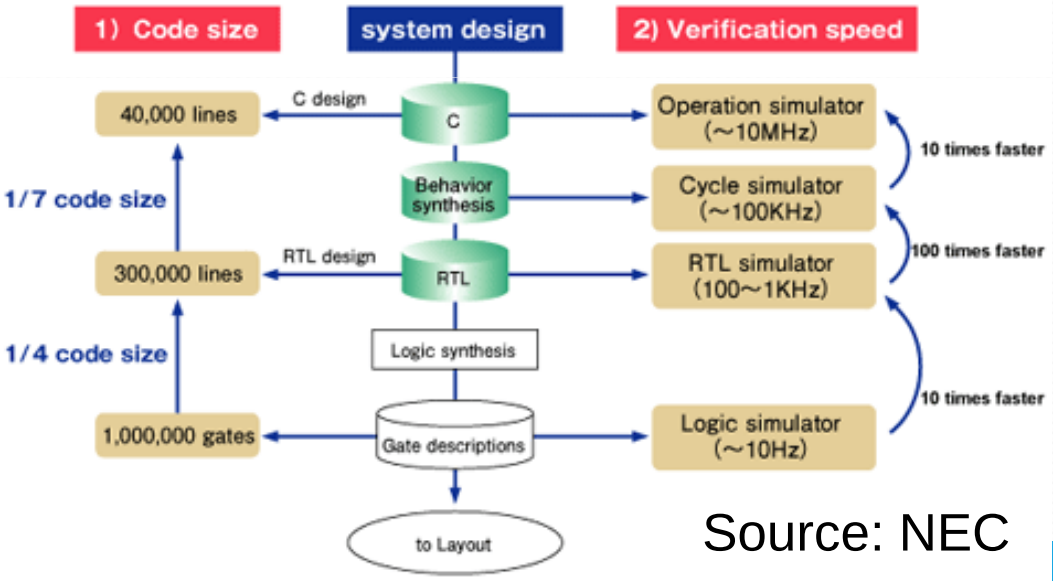


Source: NEC

NEC CyberWorkBench Reduction



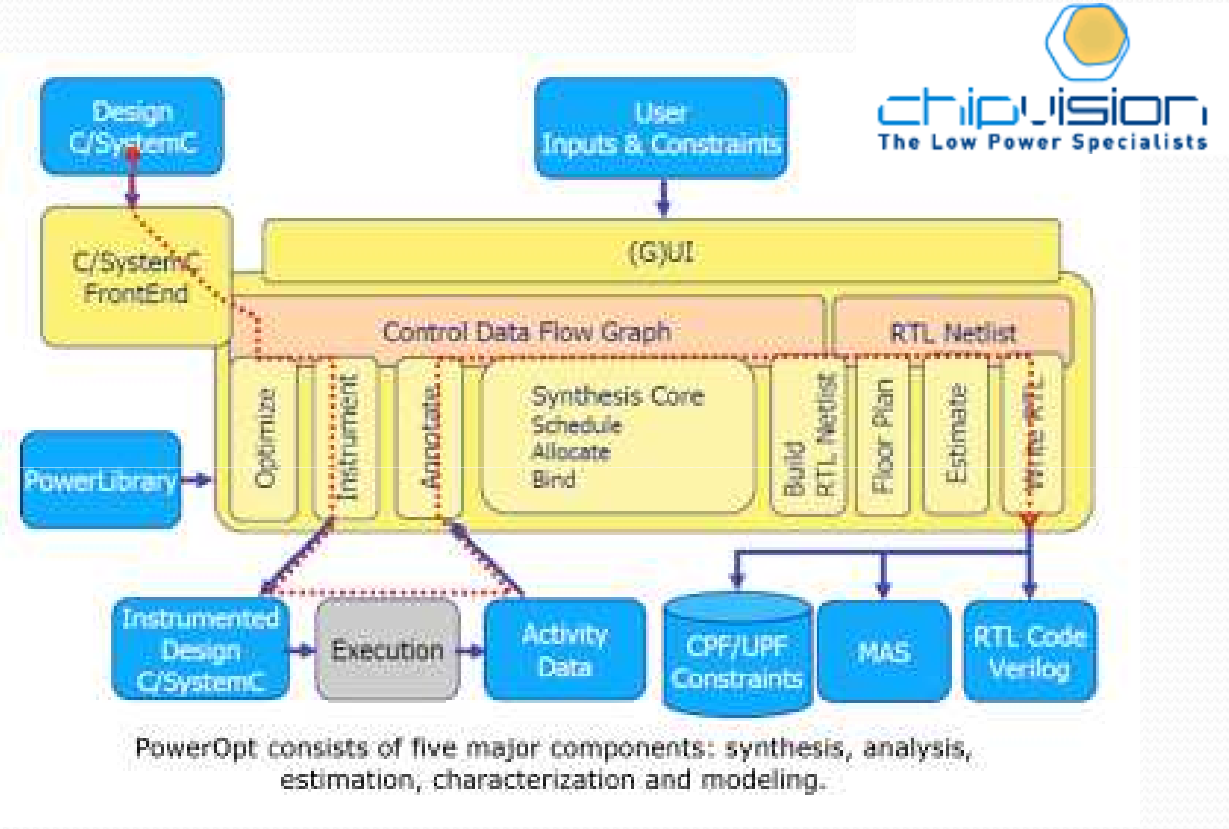




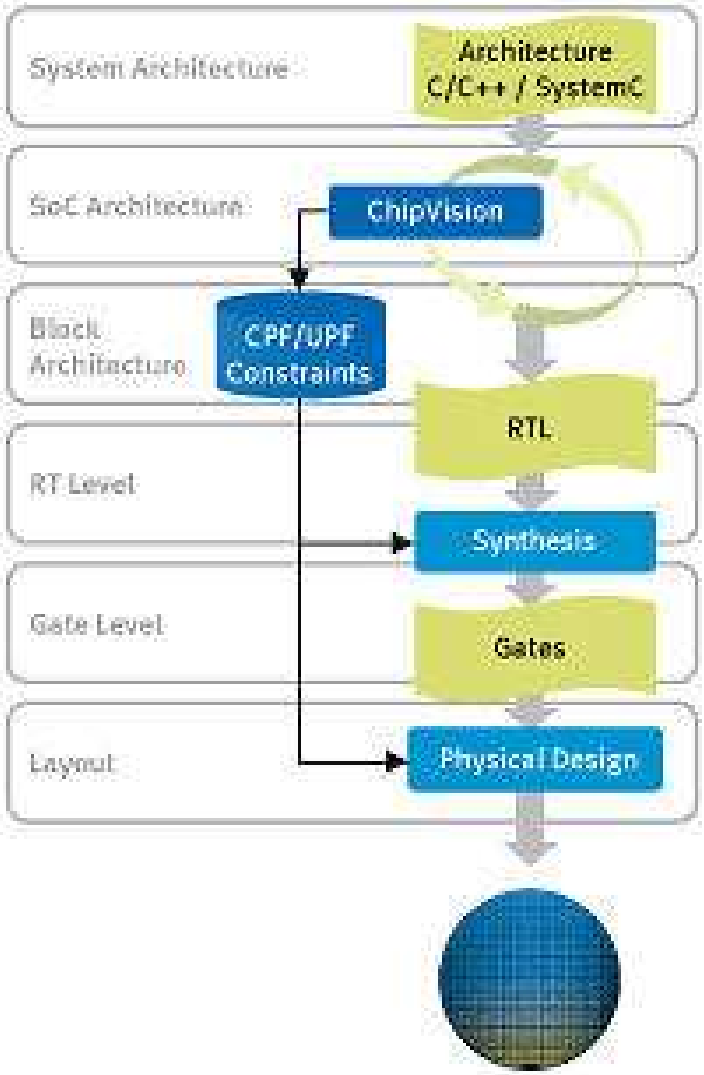
Source: NEC

ChipVision PowerOpt

- Low-power system-level tools and services provider



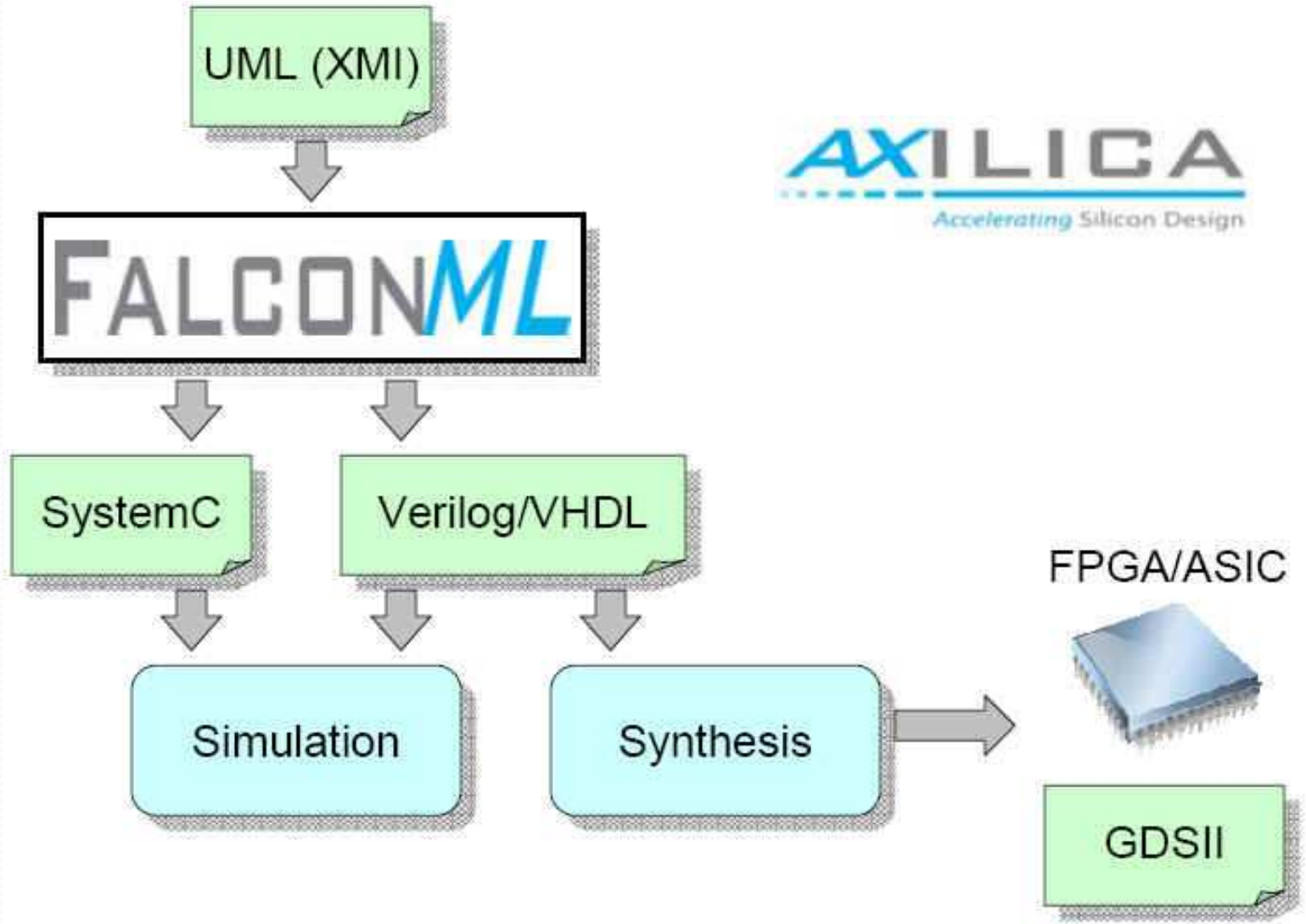
PowerOpt consists of five major components: synthesis, analysis, estimation, characterization and modeling.



Source: ChipVision

AXILICA FalconML

- UML to silicon design solution provider

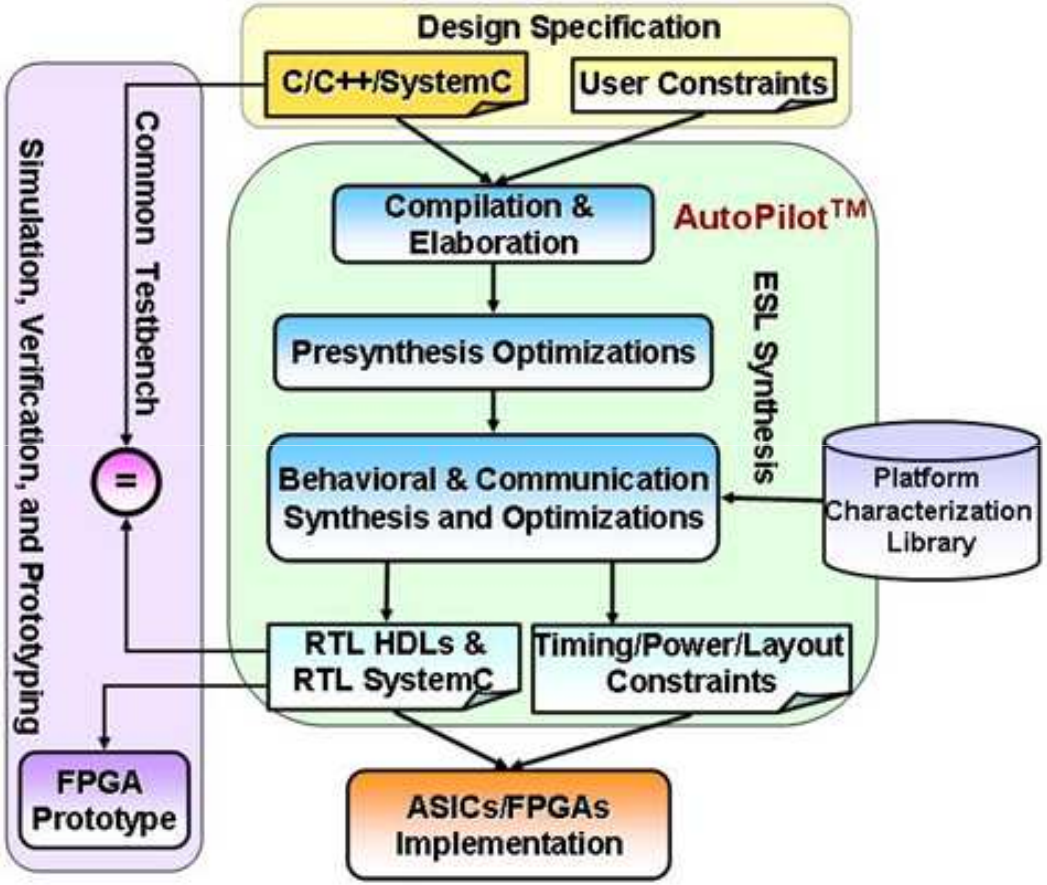


Source: AXILICA

AutoESL

- ESL to Silicon
  - Platform-based & communication-centric ESL synthesis
  - Automated ESL-to-GDSII silicon compilation
  - Rapid platform-based system-level exploration
  - More than 10X design productivity gain

AutoESL
Design Technologies, Inc.



Source: AutoESL

Others

- Open Virtual Platforms
  - OVPsim simulator: full documentation, ARM, MIPS, ORıK, homogeneous, heterogeneous, single core, multicore library
- multicore solution provider
- dedicated ESL consulting services

Summary

- Multi-core biggest challenge is debugging race issues
- Multi-core SoC performance is determined by interconnects and memory sub-systems
- 70% Top 20 companies using ESL
- ESL Hot Topics
  - High-Level Synthesis
  - ESL for Low Power
  - Design Acceleration & Emulation

"Exciting times for ESL!"

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Industrial Technology
Research Institute

Q & A

Thanks for your attention!!