積體電路設計方法

賴源泰
電機系
成功大學

積體電路時代

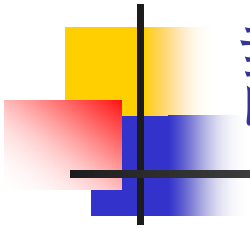
- Transistors integrated on a single chip
  - 10-100 in 1960
  - 1K-20K in 1970
  - 20K-500K in 1980
  - 10M-20M in 1990

積體電路時代

- Minimum line width in mass production
  - 5 μm in 1977
  - 2 μm in 1984
  - 1 μm in 1995
  - 0.11 μm in 2005
  - 25nm *in* 2010

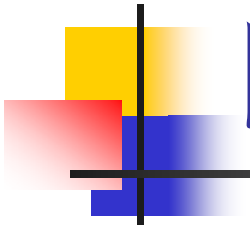
電路設計技術
Circuit Design Techniques

- PCB Circuits
  - Circuit system = ICs + Transistors + (RLC)+ PCB
- Progress in Fabrication Technology
- SSI $\Rightarrow$ LSI $\Rightarrow$ VLSI $\Rightarrow$ SOC



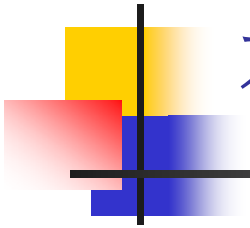
設計自動化

- Design Description
  - High level computer languages
    - Hardware Description Language
    - Verilog HDL
- Design Tools
  - Silicon Compiler (synthesizer)
  - Analyzer



階層式設計法

- Hierarchy　(Divide and Conquer)
  - Dividing a circuit into sub-circuits until they are tractable

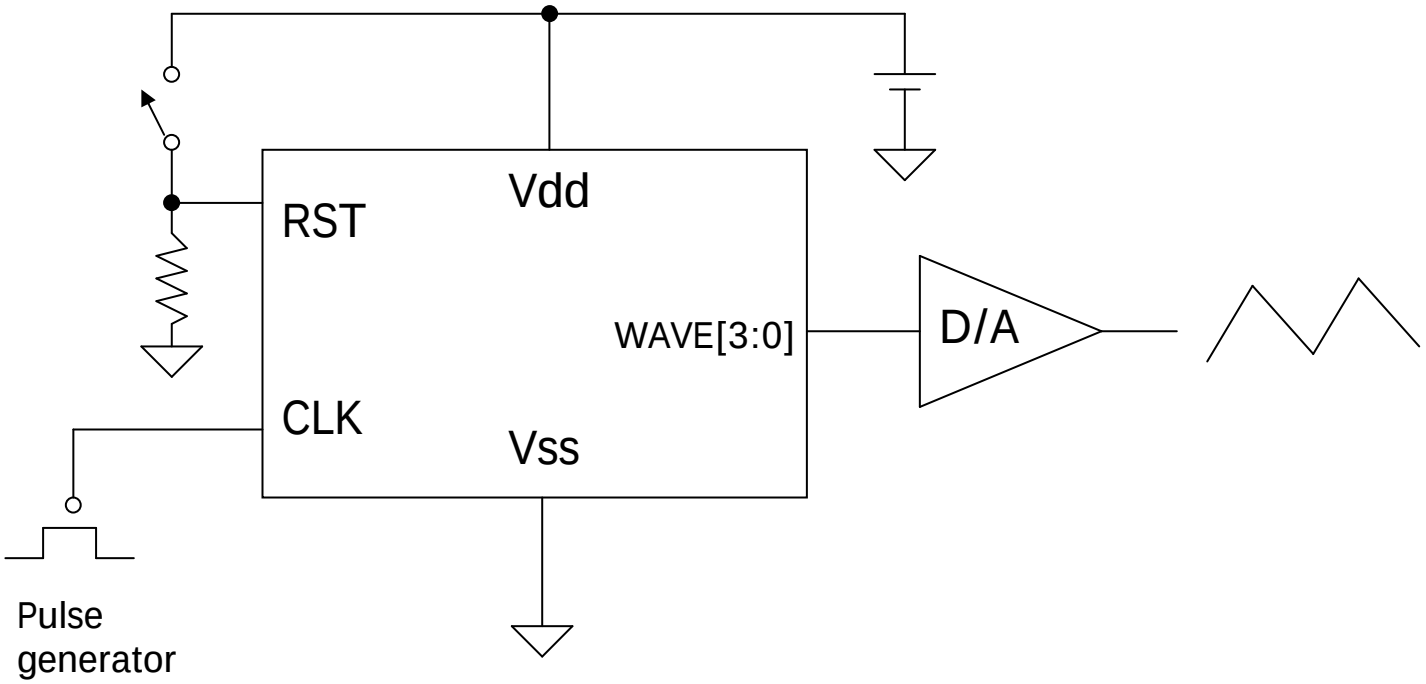


有系統的設計策略

- Structural Design Strategy
  - Behavioral Design 功能設計
  - Structural Design 結構設計
  - Physical Design 實體設計

功能設計範例
Triangle Generator1/2

- Schematic Diagram

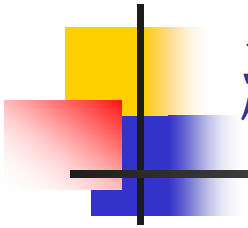


功能設計範例 Triangle Generator2/2

- Description Language

```
main(){
triangle()
}

triangle ()
{  int j=1 ;
   int I = wave = 0 ;
   while (1) {
   if (wave==15) j = -1 ;
   else if (wave == 0) j =1 ;
   wave = wave +j ;
}
```



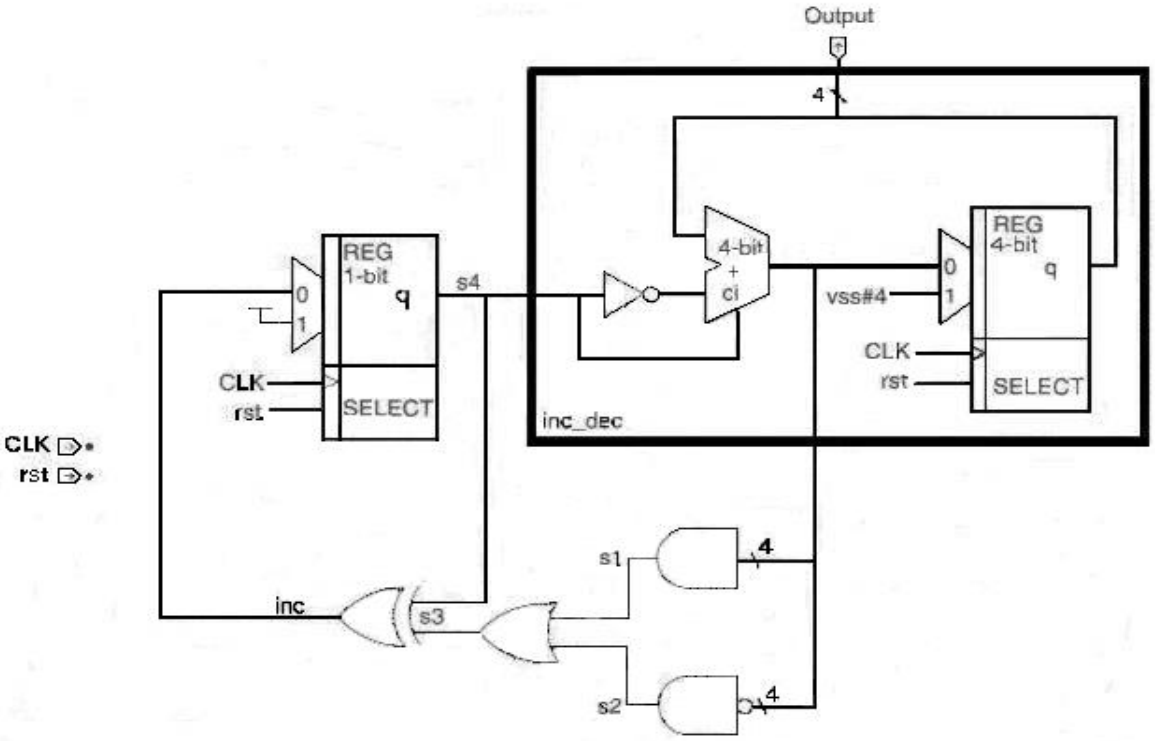
結構設計

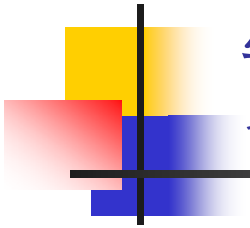
How components are interconnected to perform a certain function

- Components:
  - Registers
  - Gates
  - Functional Blocks
  - And etc.

結構設計範例
Triangle Generator1/2

- Schematic diagram





実体電路設計

- How a part is constructed to yield a specific structure and hence behavior

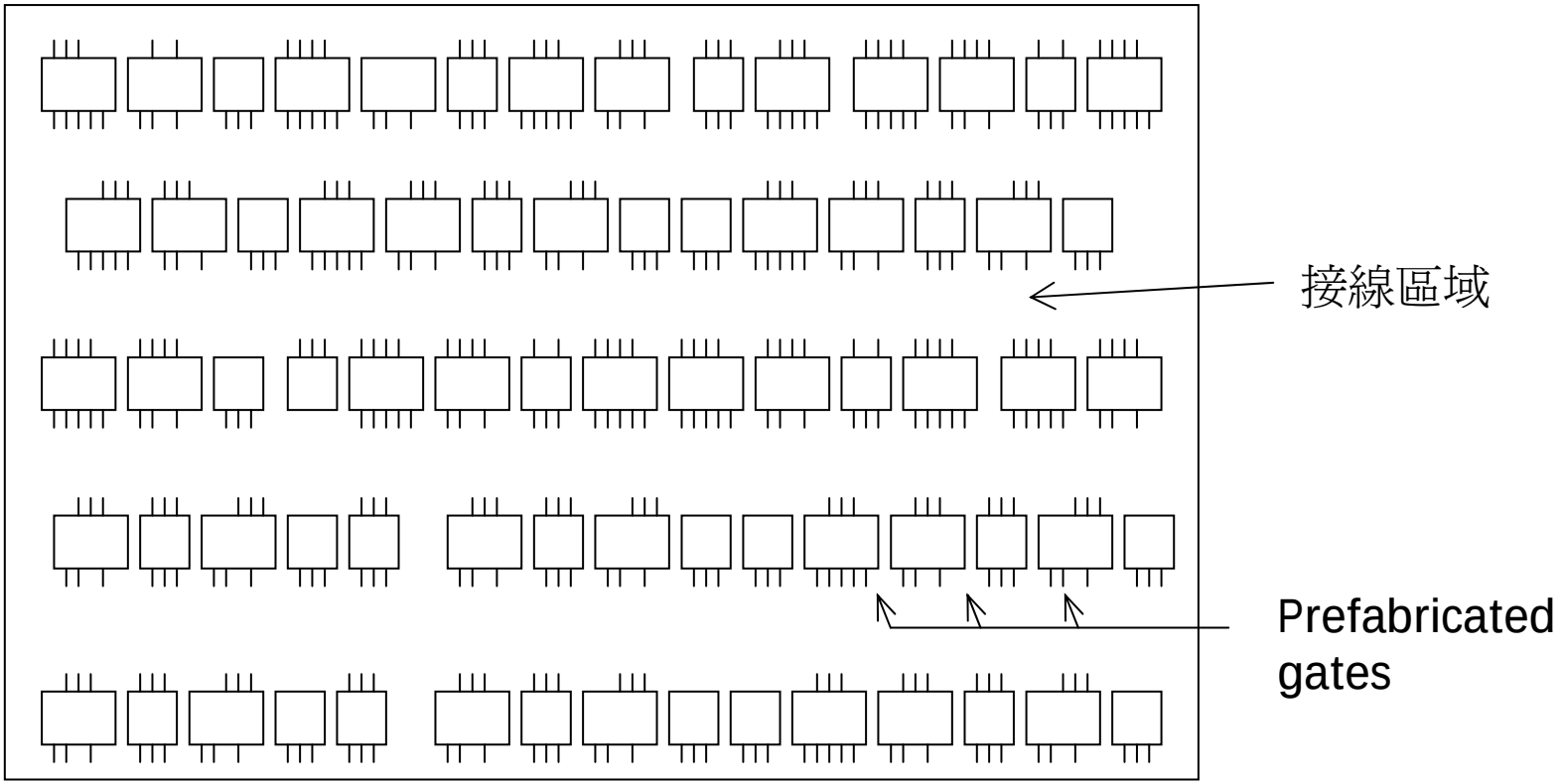
実体電路設計

- Gate Array　閘矩陣電路
- Standard Cells　標準單元組成電路
- Field Programmable Gate Array
  現場規劃閘矩陣電路
- System on a Chip　單晶片系統電路

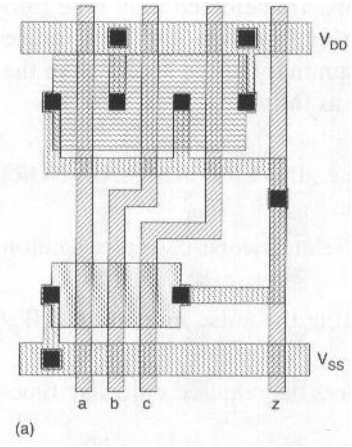
閘矩陣電路 Gate array

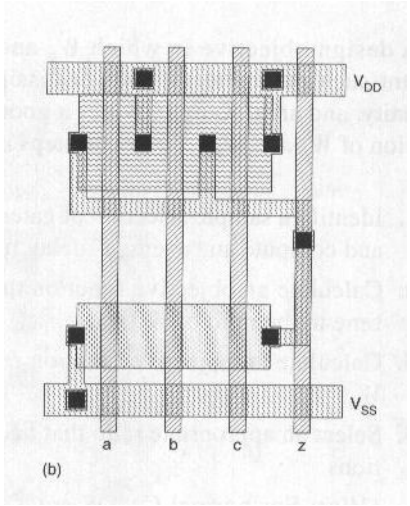
- MPGA, musk programmable gate array
  - Prefabricated primitive gates on a silicon substrate
  - Gates are connected to implement desired functions
  - Need no knowledge of detailed technology.
  - Shorter development time and lower development costs

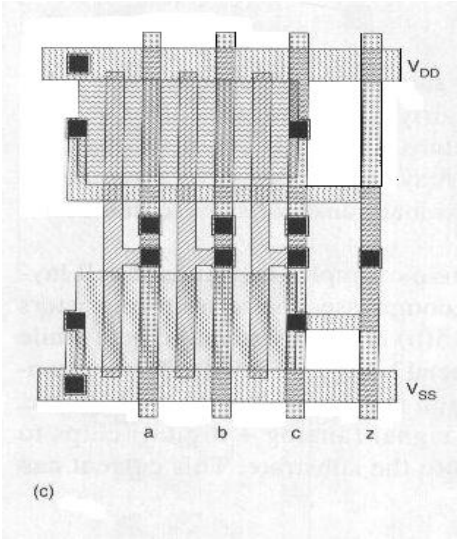
Silicon Substrate of Musk Programmable Gate Array



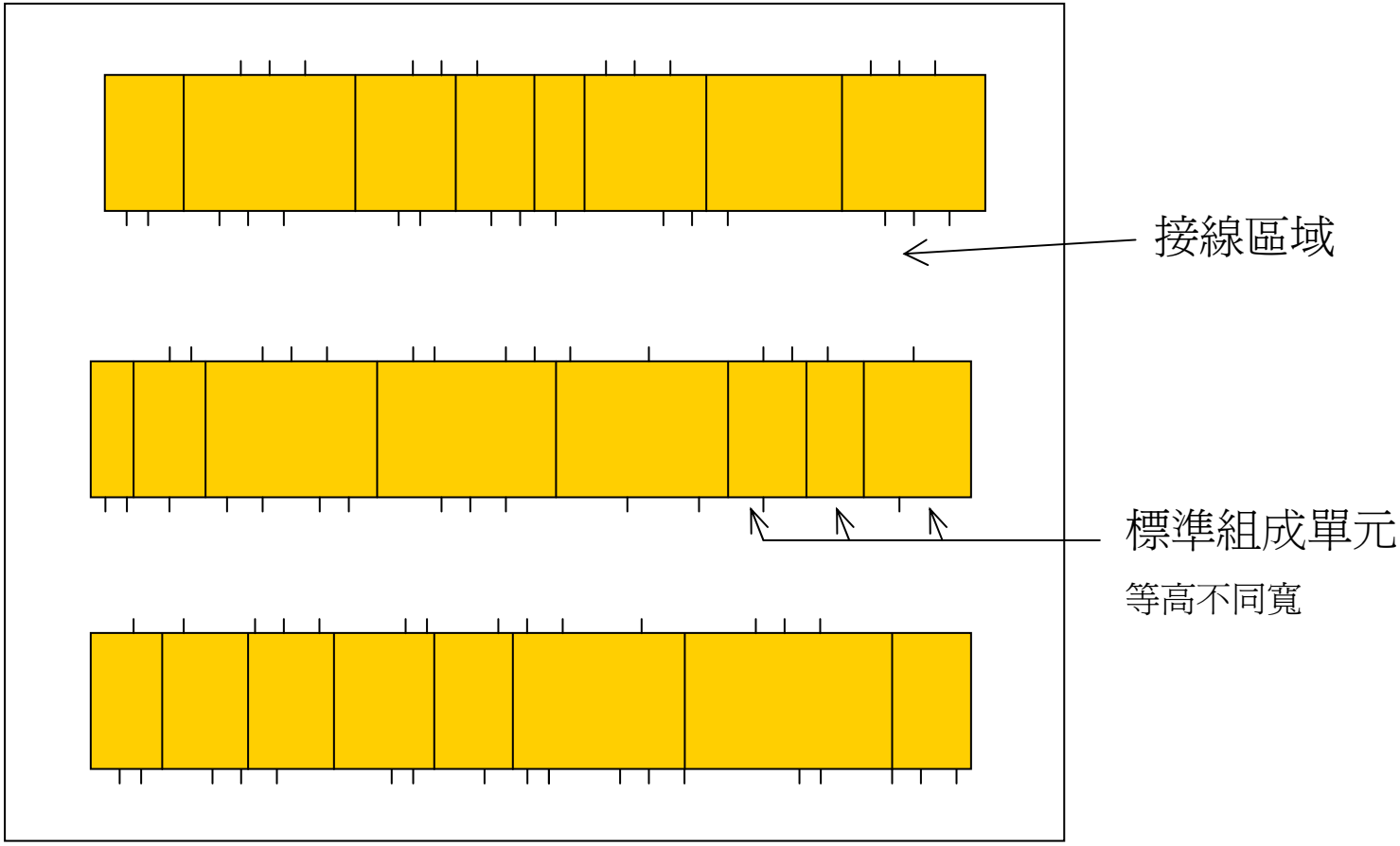
標準單元電路
Standard-cells





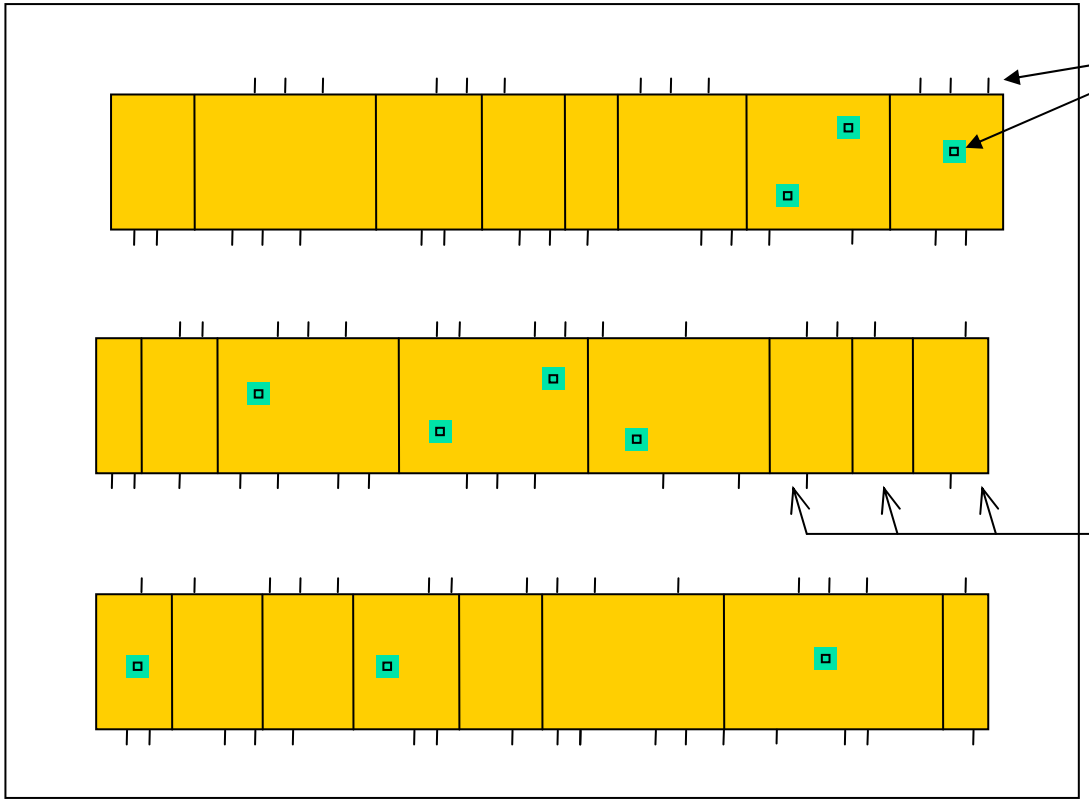


標準單元組成電路架構
Standard-cell Architecture



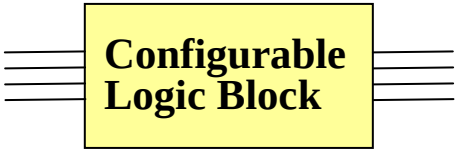
標準單元組成電路架構
Standard-cell Architecture

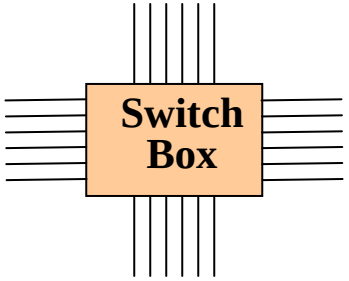
- Multiple Metal Layers



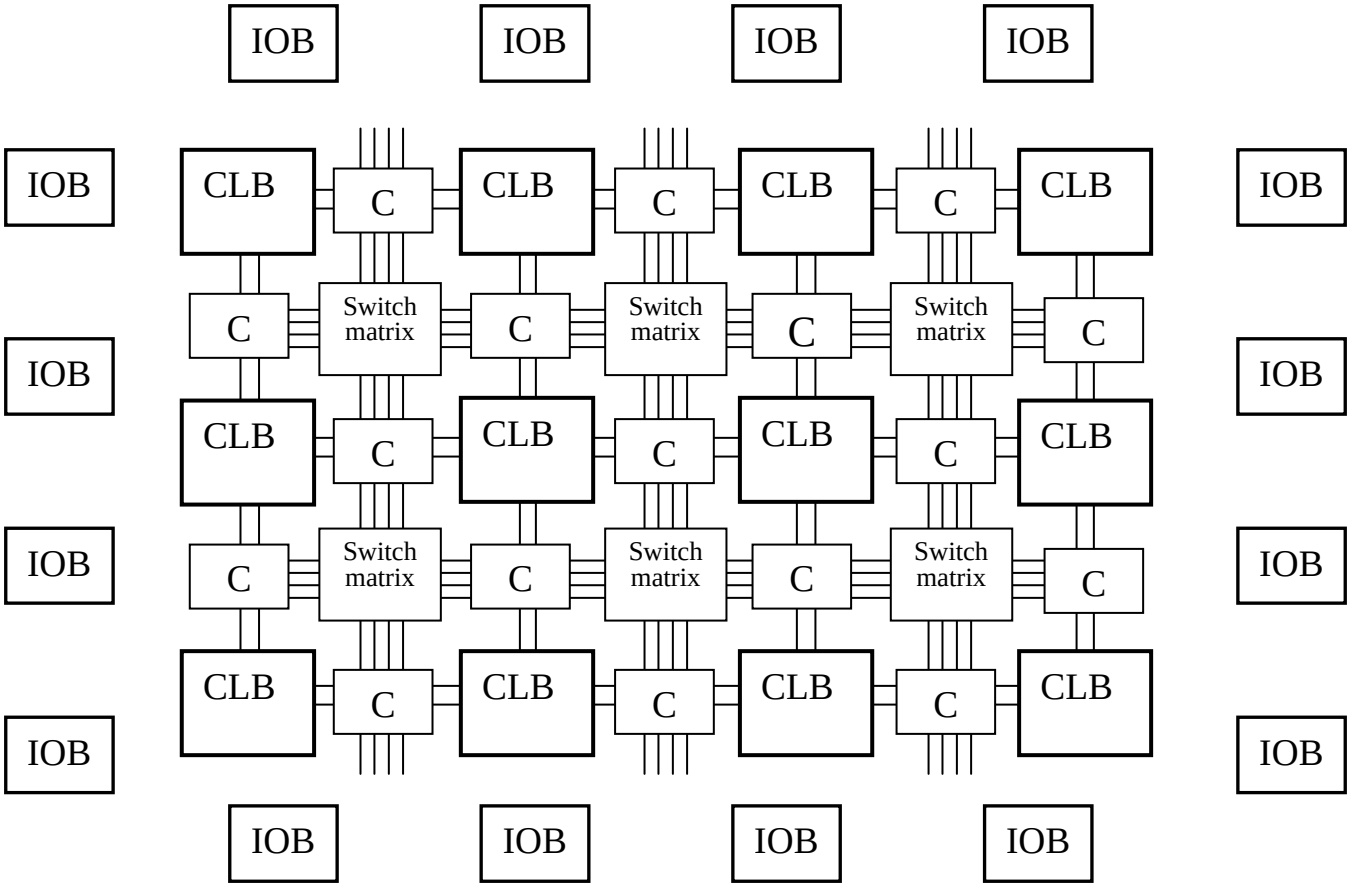
現場規劃閘矩陣電路
Field Programmable Gate Array

- Extension of
  - *Musk Programmable Gate Array*
  - *Programmable Logic Device*
- Implementation of Data Path Architecture



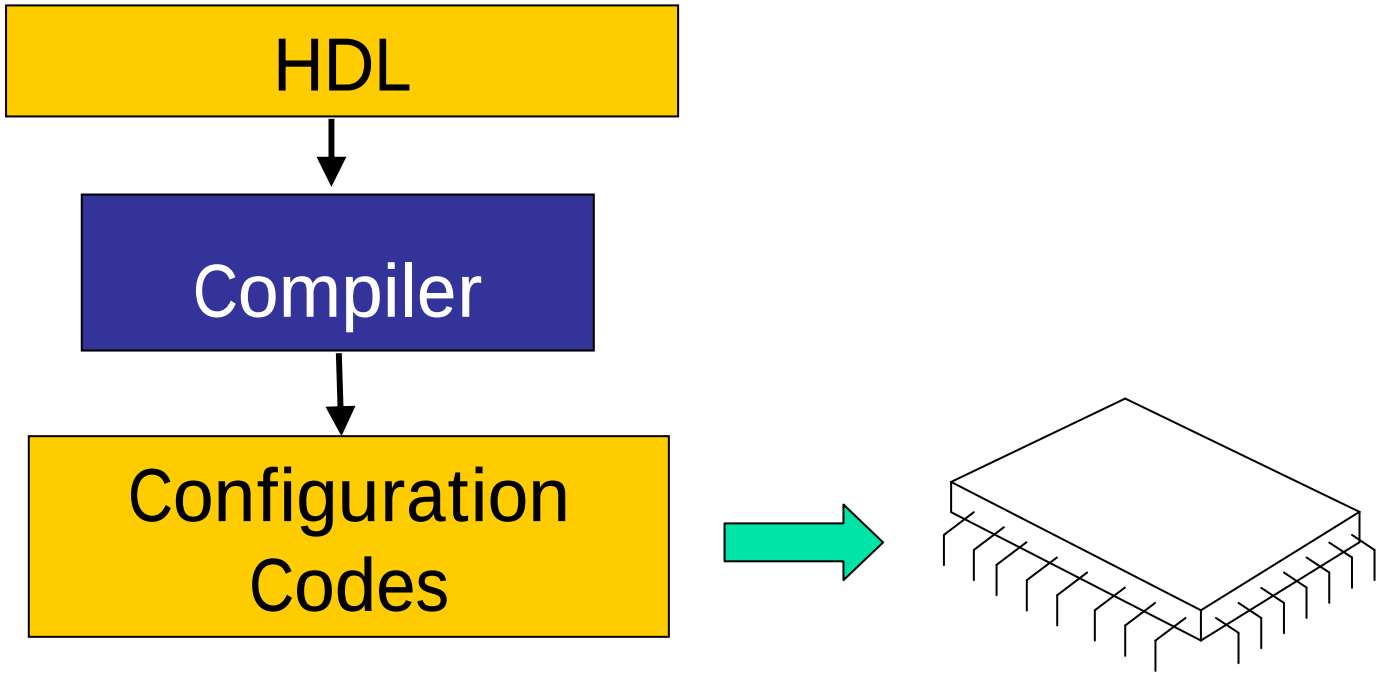


現場規劃閘矩陣電路架構
FPGA Architecture



現場規劃閘矩陣電路映對

Technology Mapping for FPGA

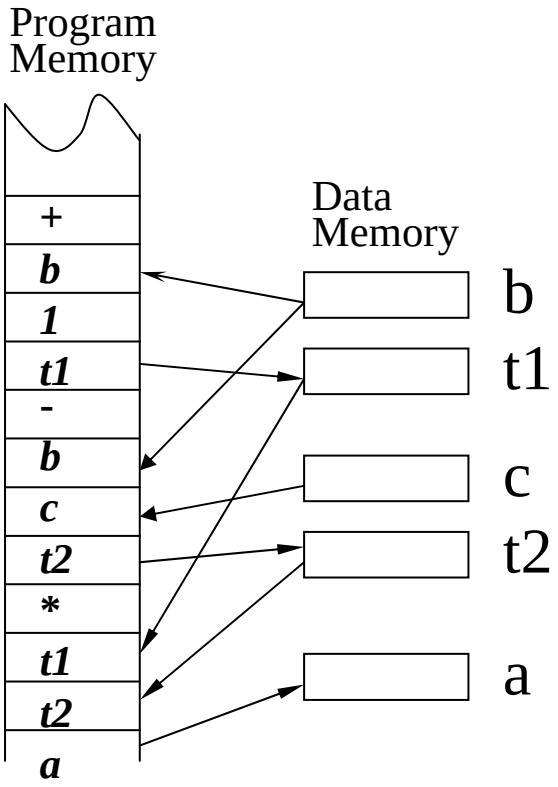


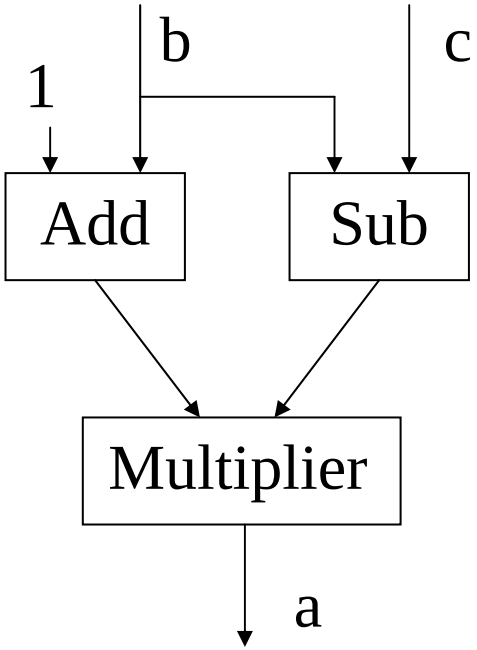
單晶片系統設計
SOC Design

- Software/Hardware Codesign Structure
- Programmable Processor + Data path

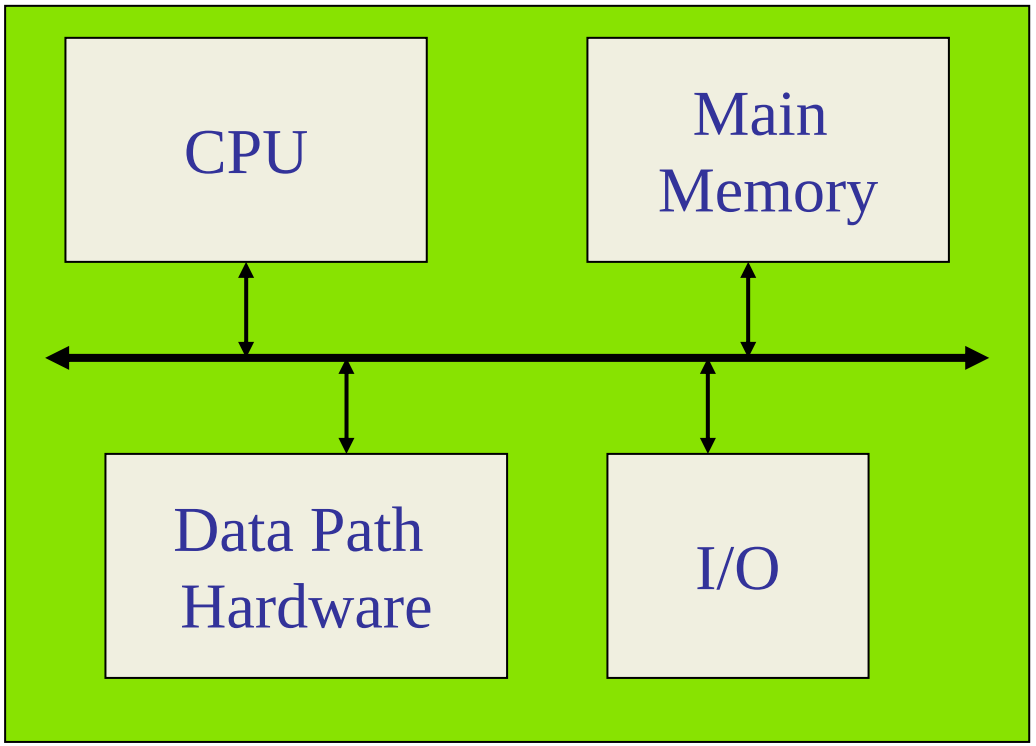
Control Flow Computation v.s. Data flow Computation

- Compute $a = (b+1)*(b-c)$

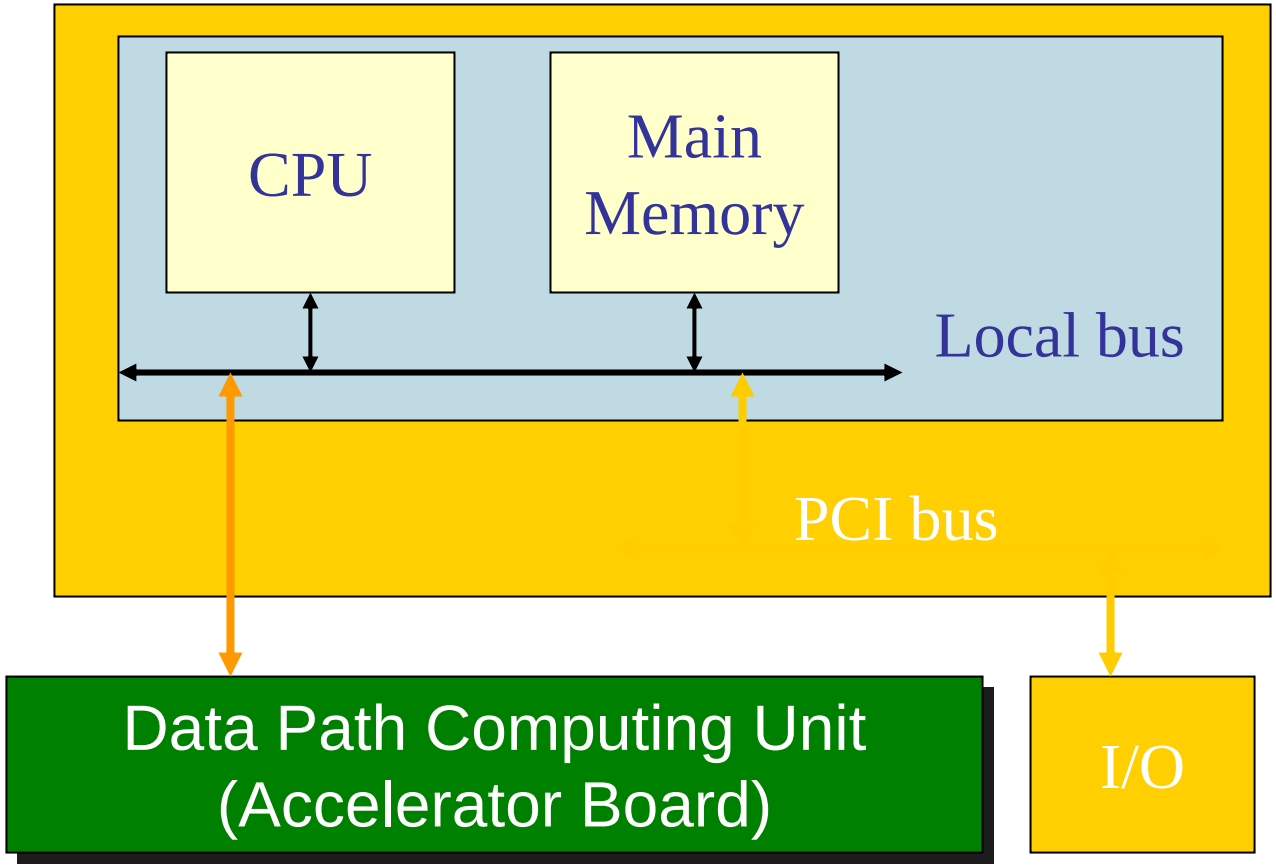




單晶片系統組織架構
Organization of SOC

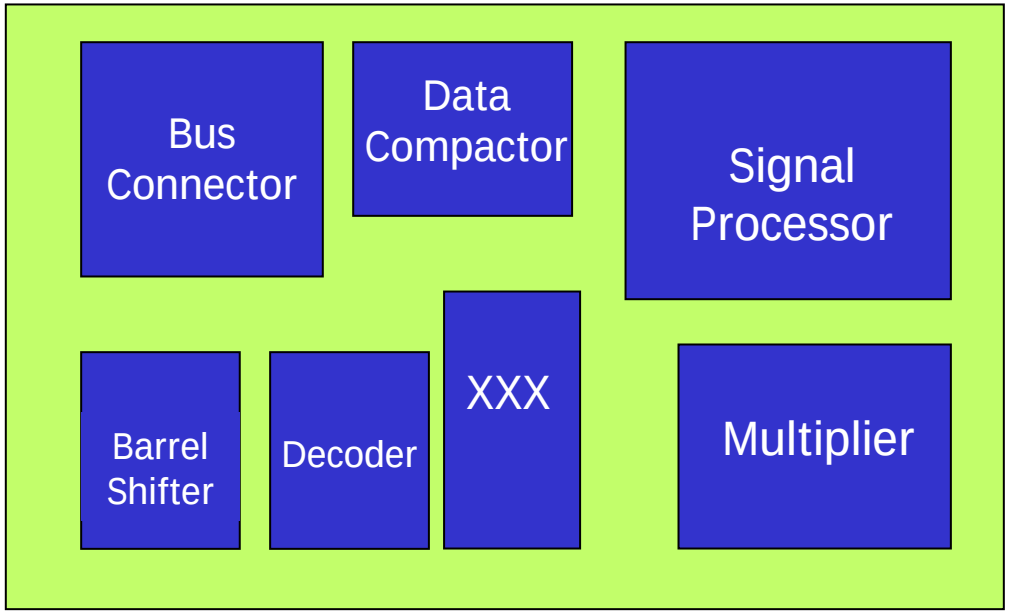


Coupling The Computing Unit to The Host

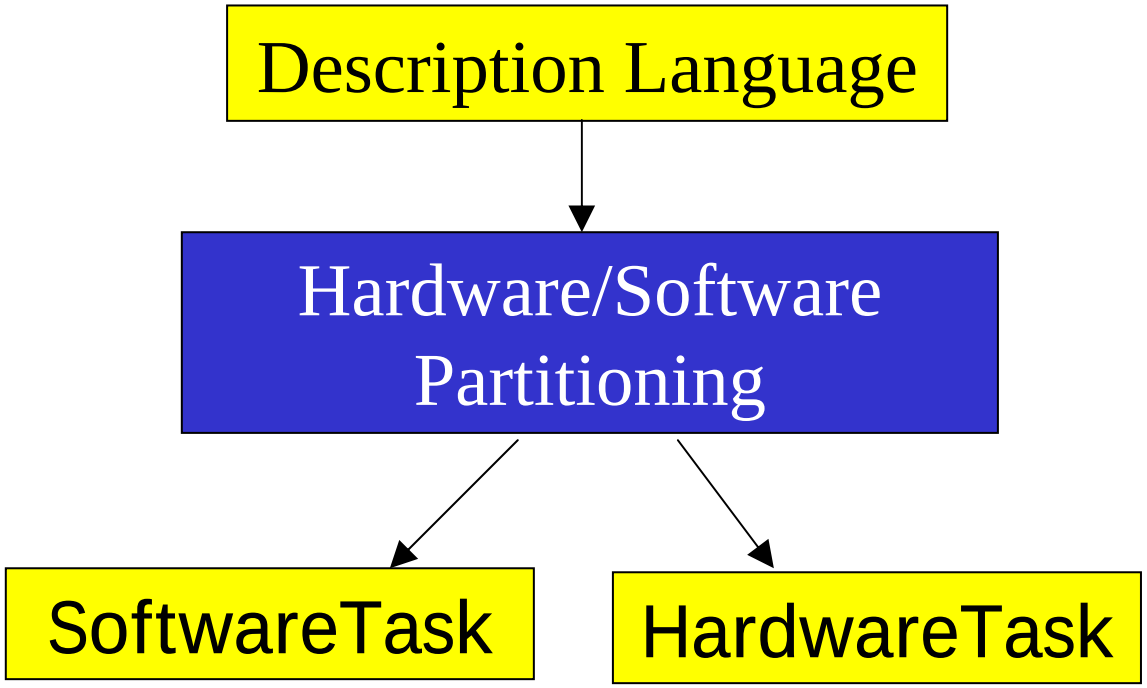


Data Path Hardware

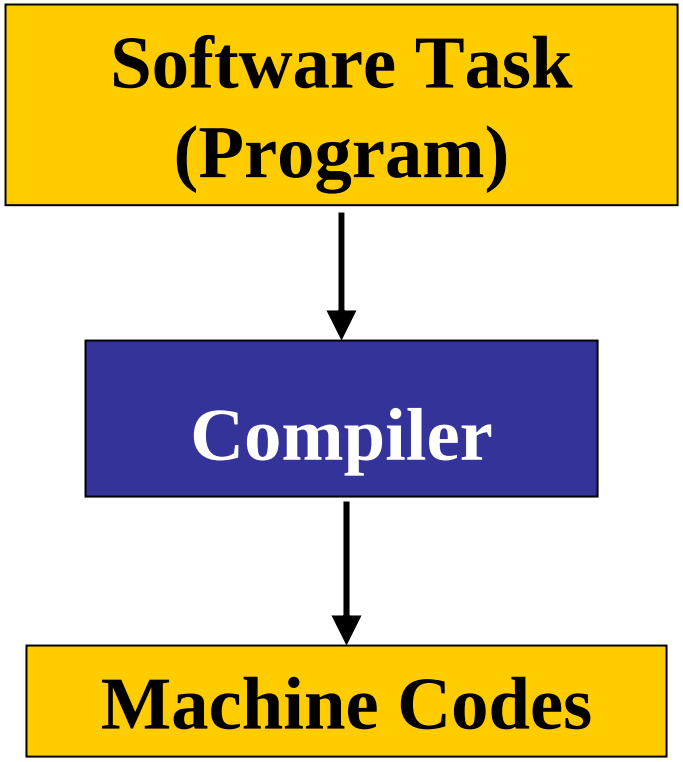
- Composed of IPs (Intellectual Properties)



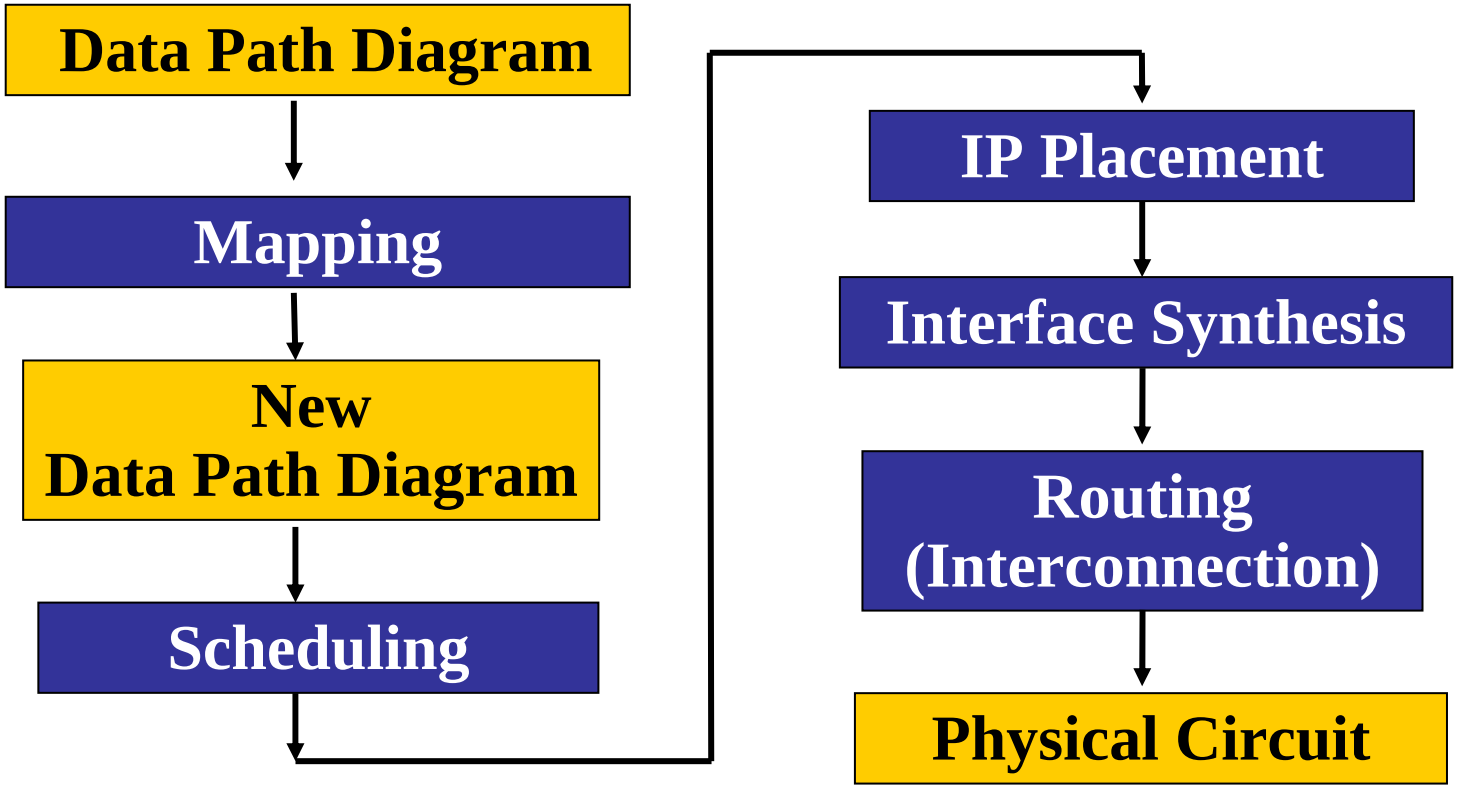
設計流程 I - 軟體硬體分工
Hardware/Software Partitioning



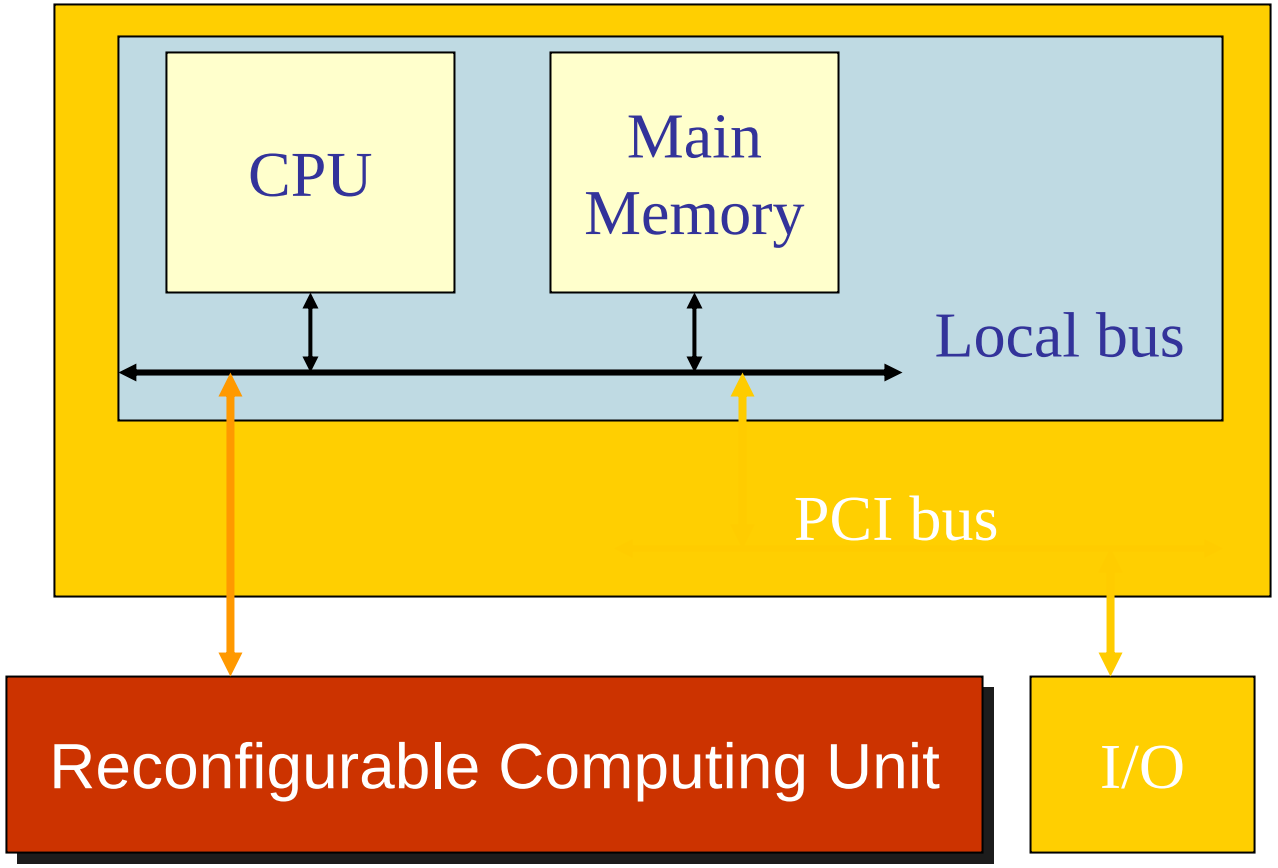
設計流程 II - 軟體編譯
Software Compilation



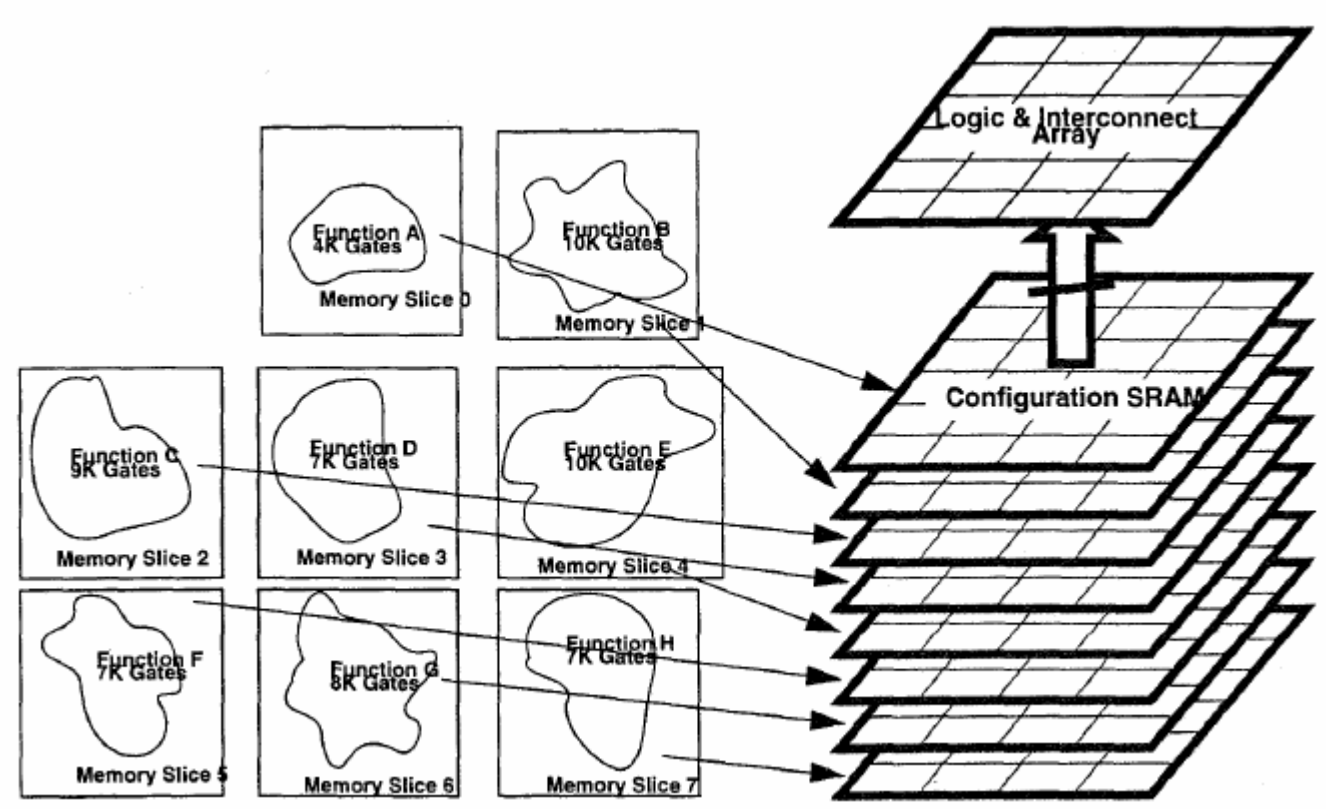
設計流程 III - 硬體設計製作
Hardware Implementation



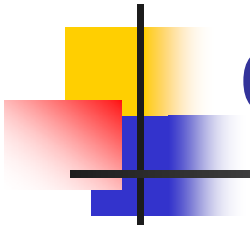
Reconfigurable Computing



Dynamic FPGA for Configurable Computing



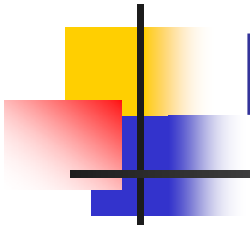
Performance of configurable computer



- One or two orders faster than processor-based computer
- Faster than Supercomputer
- Much Cheaper than Supercomputer

Product Development Cost

- Development
- Manufacturing
- Maketing sales
- General administrative
- Maintance
- Finacial



Development Cost

- Chip/circuit/physical design
- Chip integration
- Verification, test
- Software development
- EDA integration & support
- Infrastructure cost

設計技術的挑戰
Design Technology Challenges

- Design Productivity
- Minimum Power
- Manufacturability
- Reliability
- Interference

設計的產能
Design Productivity

Issues:

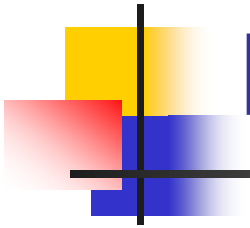
- Cost-driven design flow
- Reuse of modules, cores, RF, etc.
- Embedded software design
- Formal Verification
- Automated methods
- Heterogeneous component integration

低耗電
Low Power Design

- Portable System
- Low Voltage
- Low Power
- Power management

可製造的設計
Design for Manufacturability

- Performance/power variability
- Device parameter variability
- Lithography limitations impact on design
- Mixed signal Design for testability
- Mask cost
- System level reliability
- Thermal Built-in-self-test



Reliability

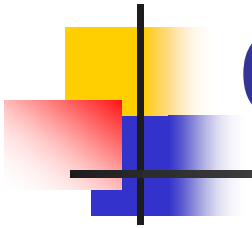
- Logic/Circuit/Layout: mean-time-to-failure aware design
- Built-in self repair
- Software reliability
- Robust design

介面設計
Design of interference

- Logic/circuit/layout: signal integrity analysis
- Eletromagnetic interference analysis
- Thermal analysis
- Interference of heterogeneous components (optical, mechanical, bio, etc.)

高速系統
High Performance System

- Video Image Processing
- Accelerators for Combinatorial Problems
- DNA Sequence Matching
- Cryptographic attacks
- Scientific Computation
- Simulation Engines



Conclusions

- Miniature
- High Circuit Density
- Complex System
- High design complexity
- Challenge design work