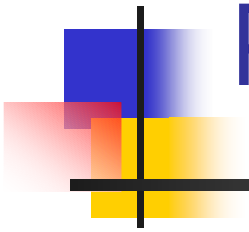
晶片設計產業發展現況與展望

國立雲林科技大學電機工程系

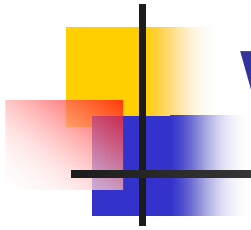
陳春僥

November 7, 2006



Part I

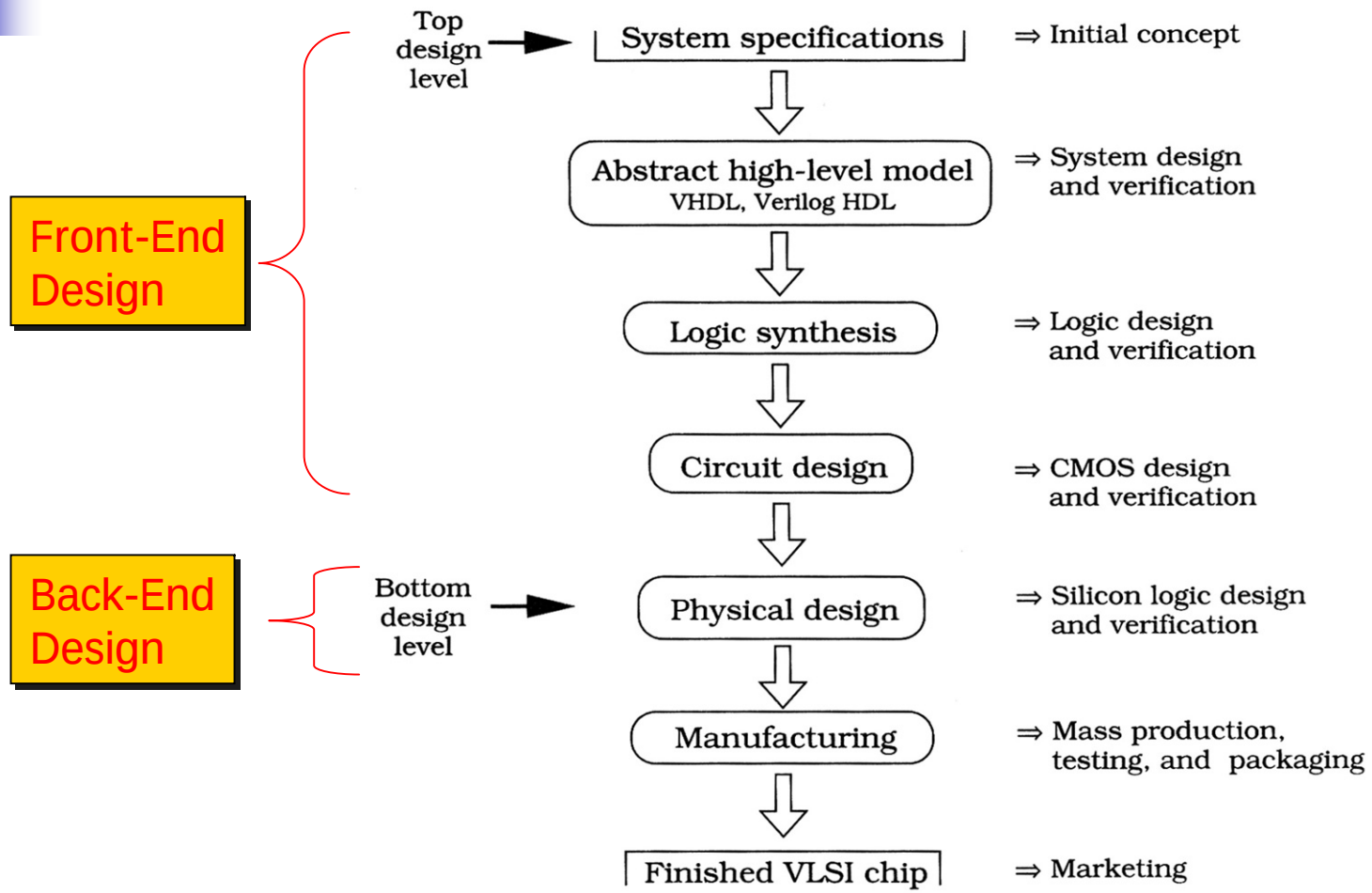
VLSI 是什麼?



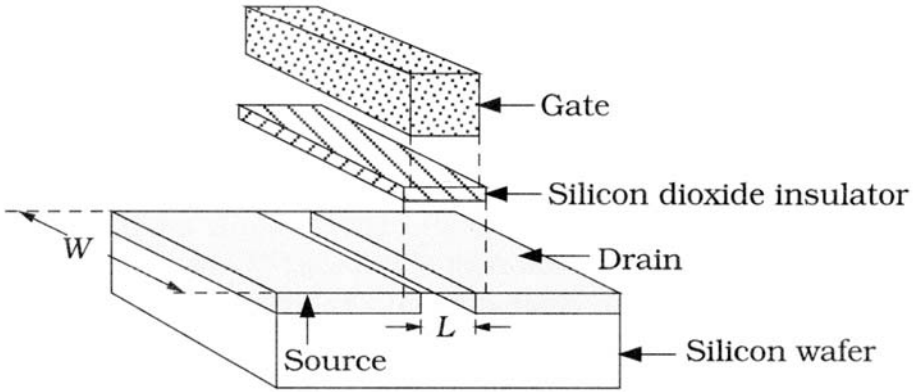
What is VLSI?

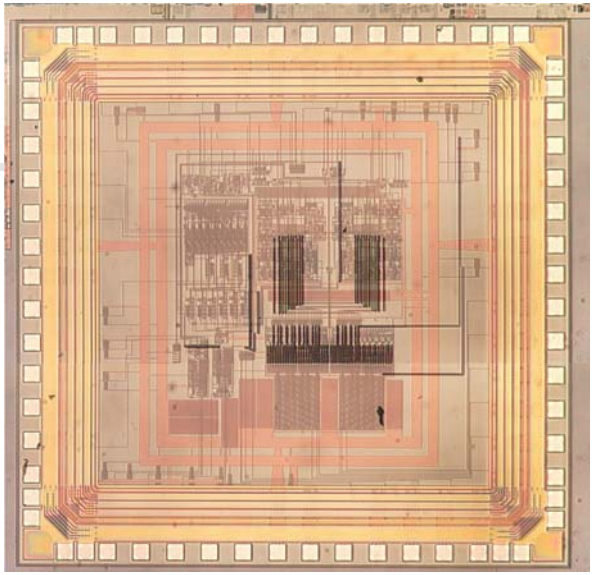
- VLSI—
  - **V**ery-**L**arge-**S**cale **I**ntegration
  - 超大型積體電路
  - 1,000,000個電晶體以上
  - 晶片層次的設計
- PCB—
  - 分立元件
  - 電路板層次的設計

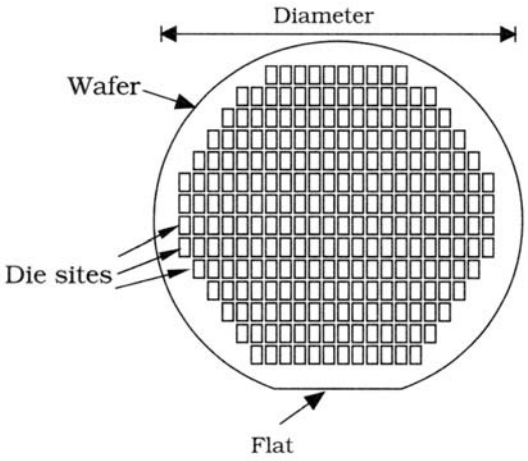
設計之層次

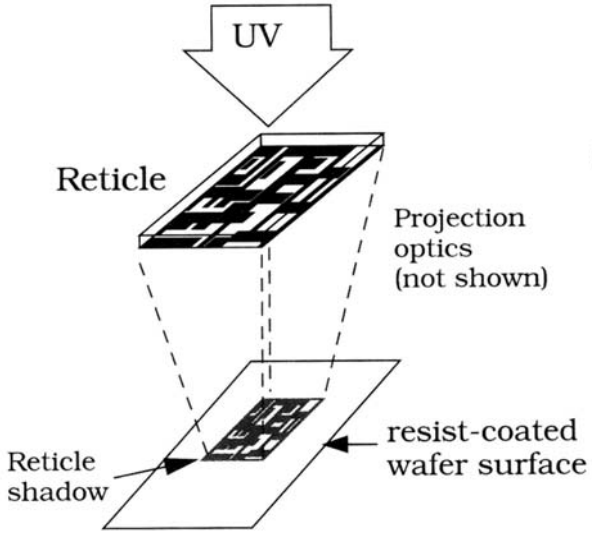

Front-End Design
Back-End Design
Top design level
Bottom design level
System specifications
⇒ Initial concept
Abstract high-level model
VHDL, Verilog HDL
⇒ System design and verification
Logic synthesis
⇒ Logic design and verification
Circuit design
⇒ CMOS design and verification
Physical design
⇒ Silicon logic design and verification
Manufacturing
⇒ Mass production, testing, and packaging
Finished VLSI chip
⇒ Marketing

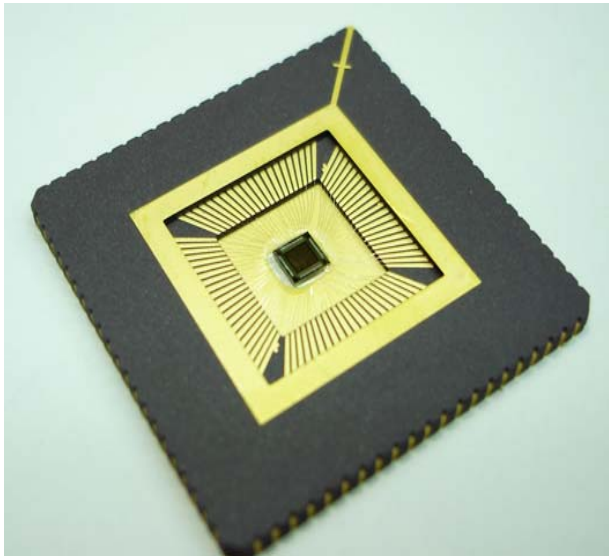
Transistor, Wafer, Die, & Chip









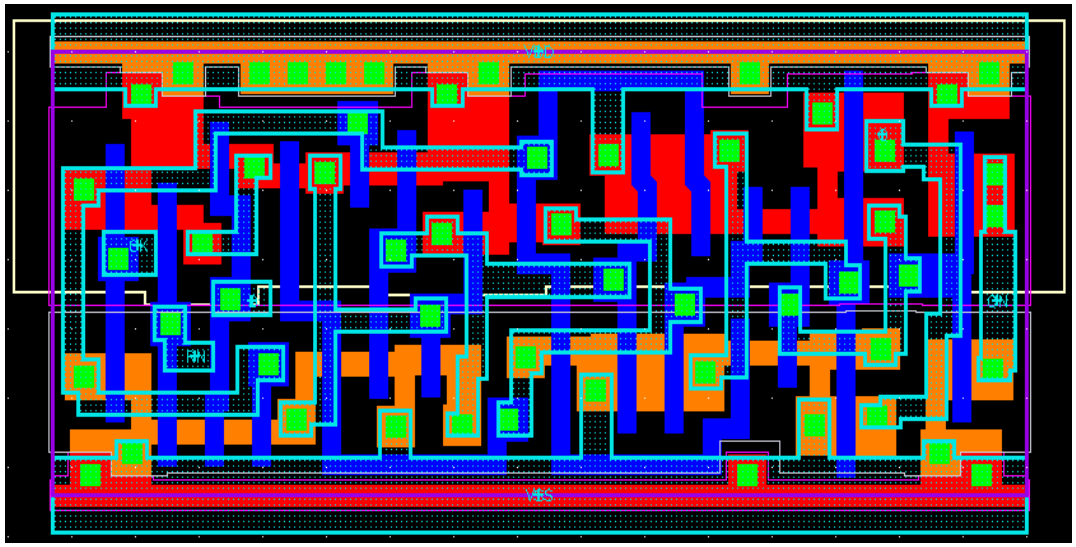


VLSI 晶片之設計型態

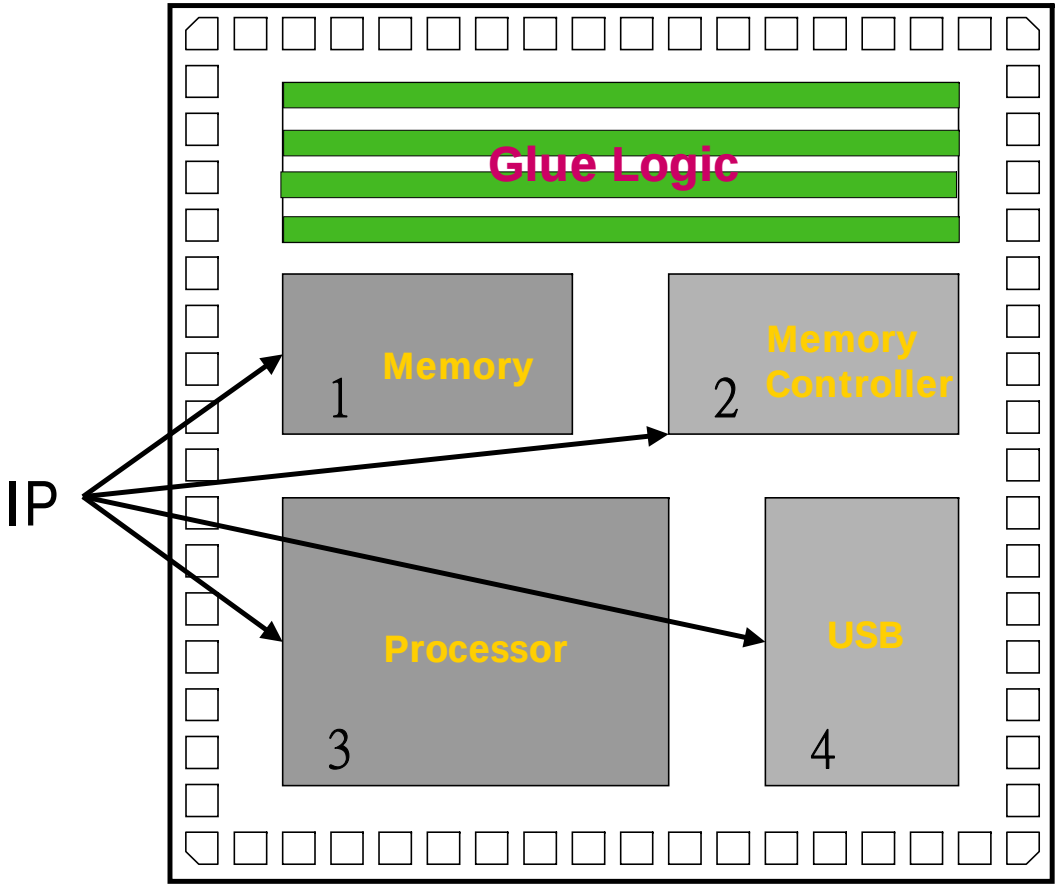
- Full Custom Design (客制式)
- Cell (IP) Based Design (元件庫式)
- Semi-Custom Design (半客制式)
- ASIC—
  - Application-Specific Integrated Circuit

設計型態

- Every circuit is custom designed for the project
- Analog circuit, standard cell library design, I/O
- Highest chip density & design flexibility
- Long development time

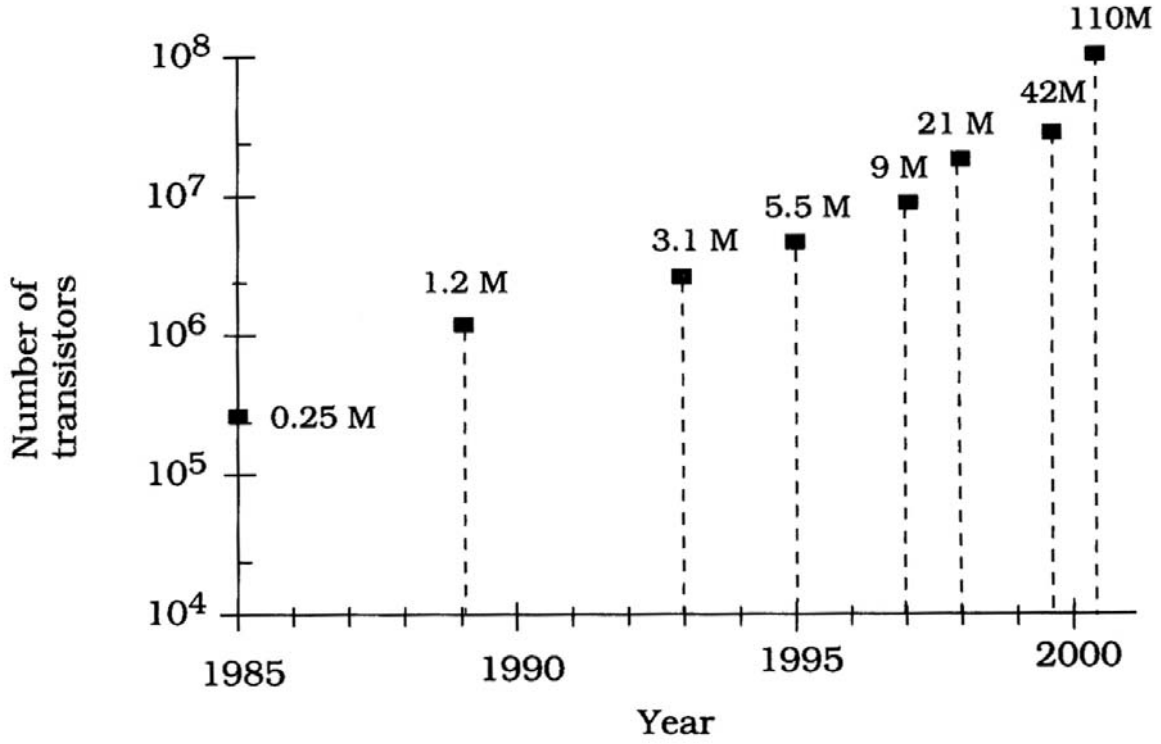


Cell (IP) Based Design



Moore's Law

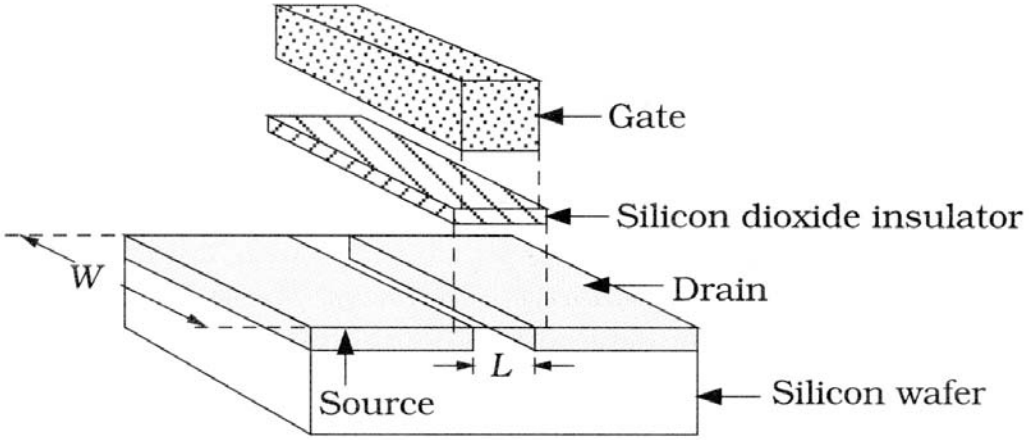
- The number of transistors on a chip would double about every 18 months.



Technology Evolution

	1995	1996	1998	1999	2001
Process Technology	0.8um	0.6um	0.25um	0.18um	0.15um

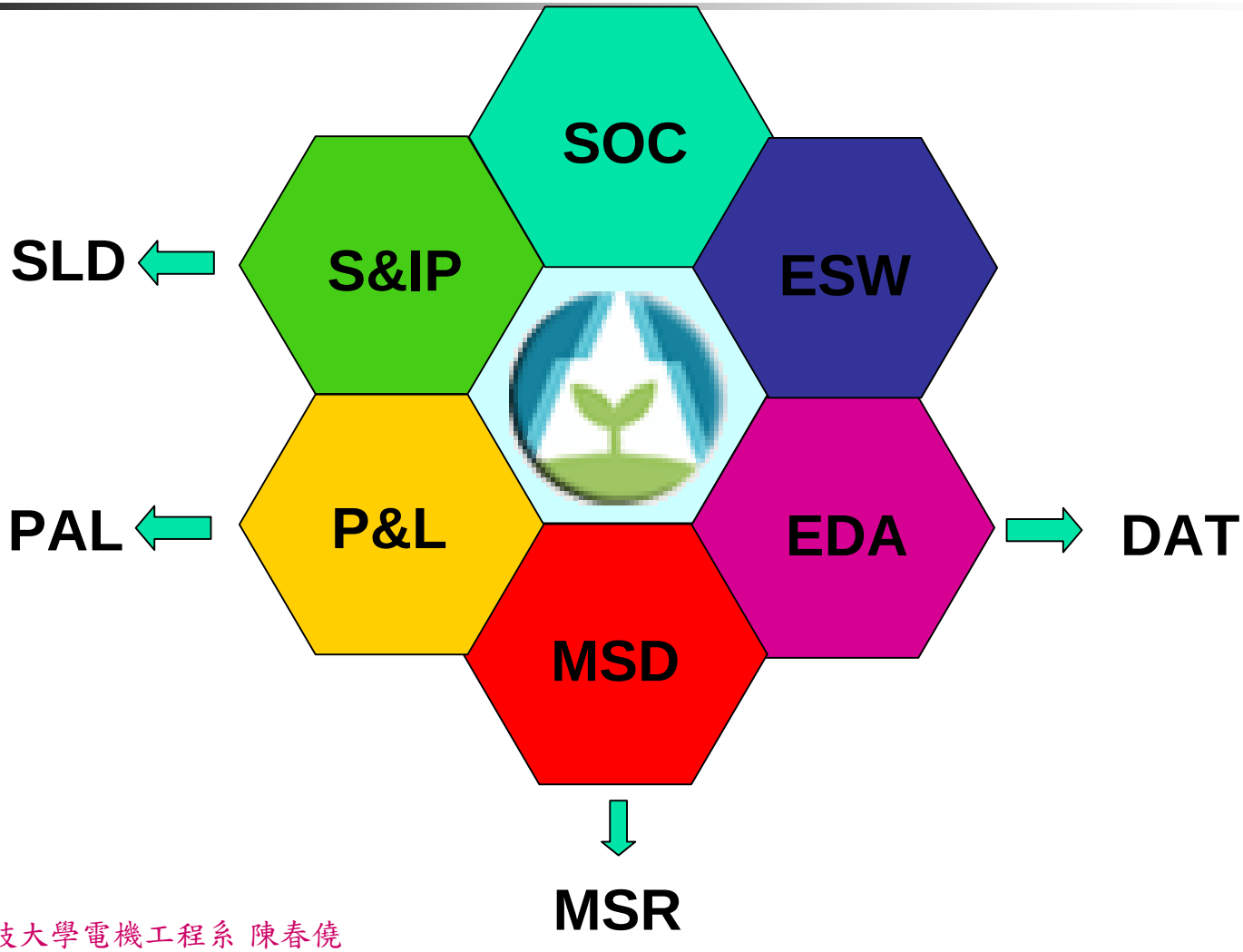
Moore's Law

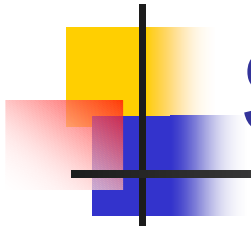


Part II

六大聯盟與研究領域

6 Consortia



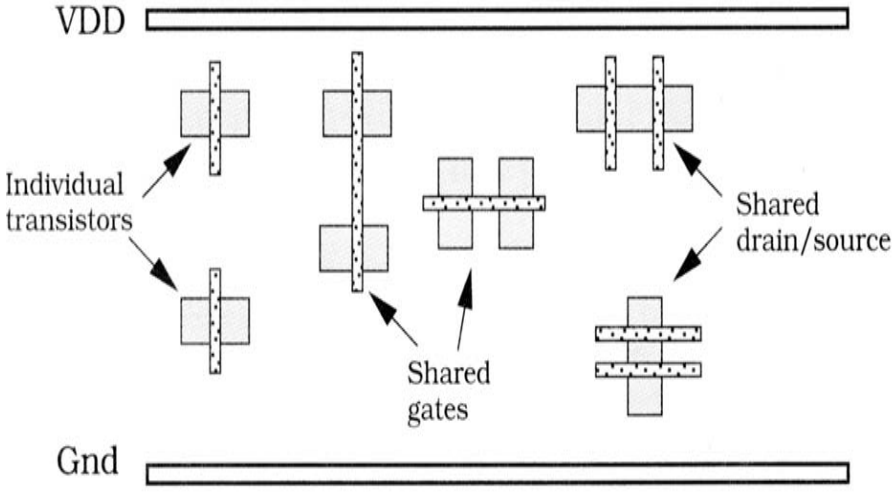


S&IP Consortium

- S&IP—
  - **S**ystem-on-a-Chip (SoC)
    - IP-based SoC
    - Plateform-based SoC
  - Digital **I**ntellectual **P**roperty (DIP)
    - Soft IP— synthesizable RTL code + script
    - Firm IP— netlist + placement information
    - Hard IP— GDSII file (analog block)

P&L Consortium

- P&L—
  - **P**rototyping (Rapid-Prototyping System, RPS)
    - FPGA— logic
    - SoPC— logic + processor → SW/HW co-design
  - **L**ayout
    - Analog IC layout
    - Mixed-signal IC layout



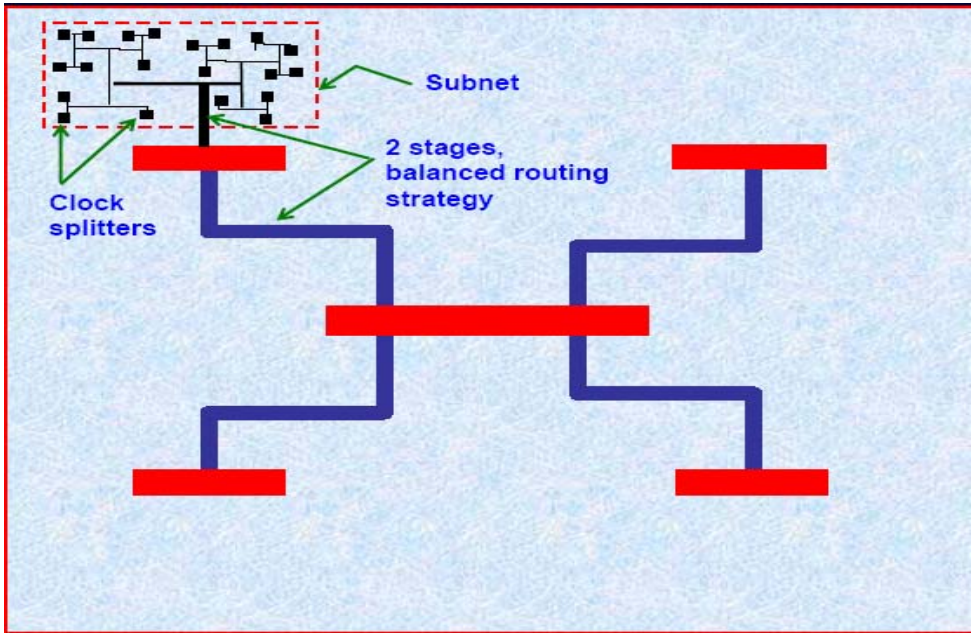
MSD Consortium

- MSD—
  - **M**ixed-**S**ignal **D**esign
    - Analog (current-mode, voltage-mode)
    - Analog + Digital

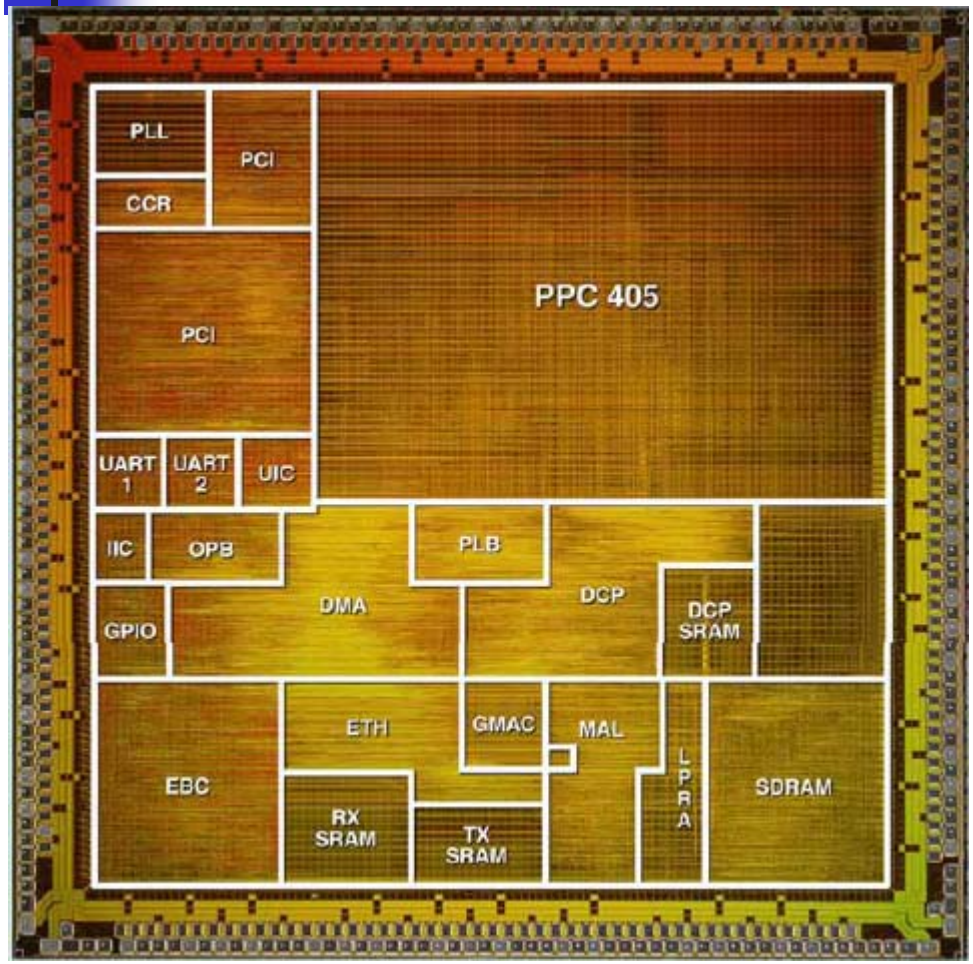
    → OPAMP, ADC, DAC, PLL, …
  - MEMS (Micro-Electro-Mechanical Systems)
    - Biochip
  - Power IC
    - Regulator
  - RF IC
  - Nano-meter Circuit Design

EDA Consortium

- EDA—
  - **E**lectronic **D**esign **A**utomation
  - Also called “CAD” (Computer-Aided Design)
  - Placement & Routing
  - Testing
    - Testable design (DfT)
  - Signal Integrality
    - X-talk, IR drop
  - Low Power
    - Multi-VT, Multi-VDD



What is an SoC?

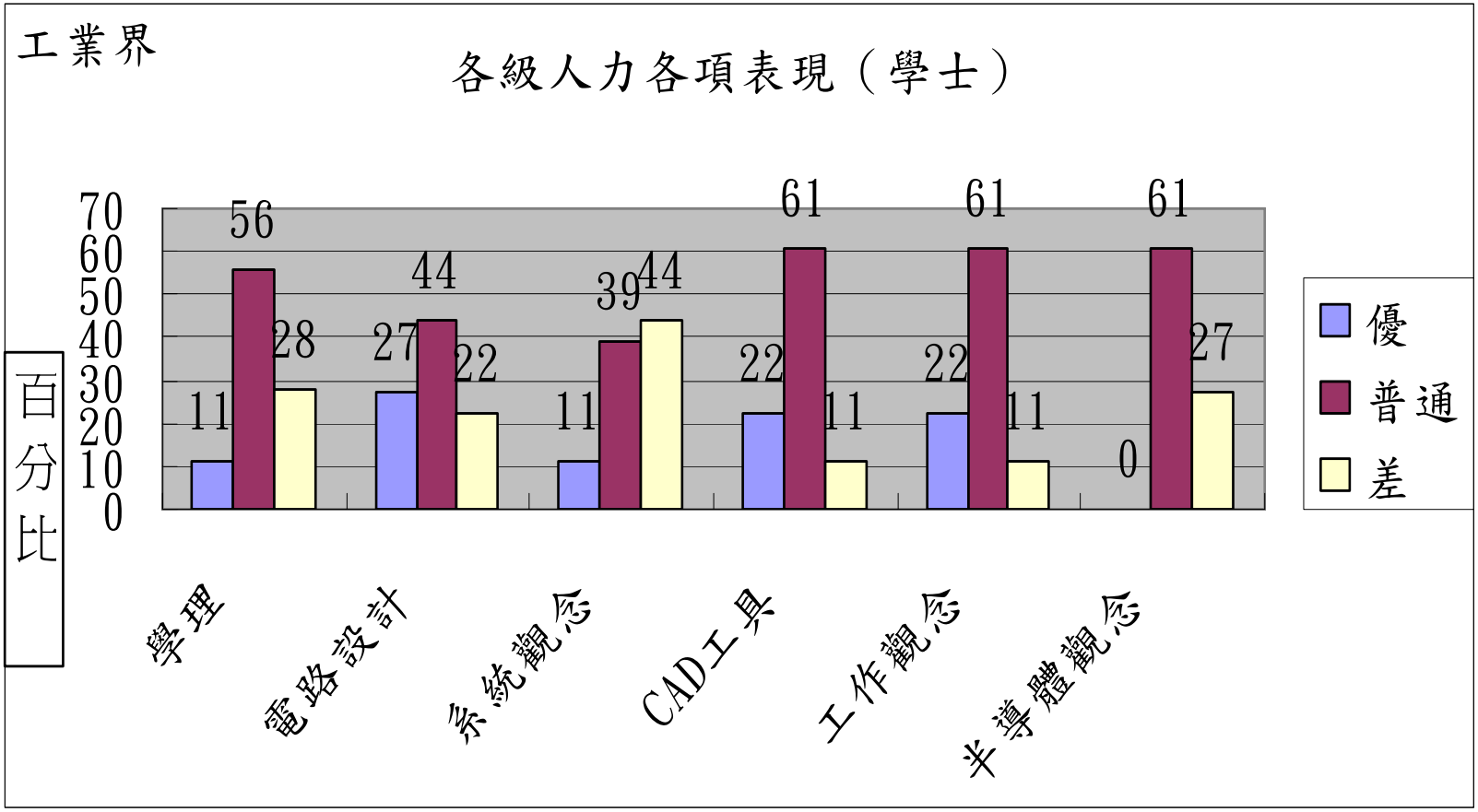


- An SoC contains:
  - Portable / reusable IP
  - Embedded CPU
  - Embedded Memory
  - Real World Interfaces (USB, PCI, Ethernet)
  - Software (both on-chip and off)
  - Mixed-signal Blocks
  - Programmable HW (FPGAs)
  - > 500K gates
- Technology: 0.25um and below

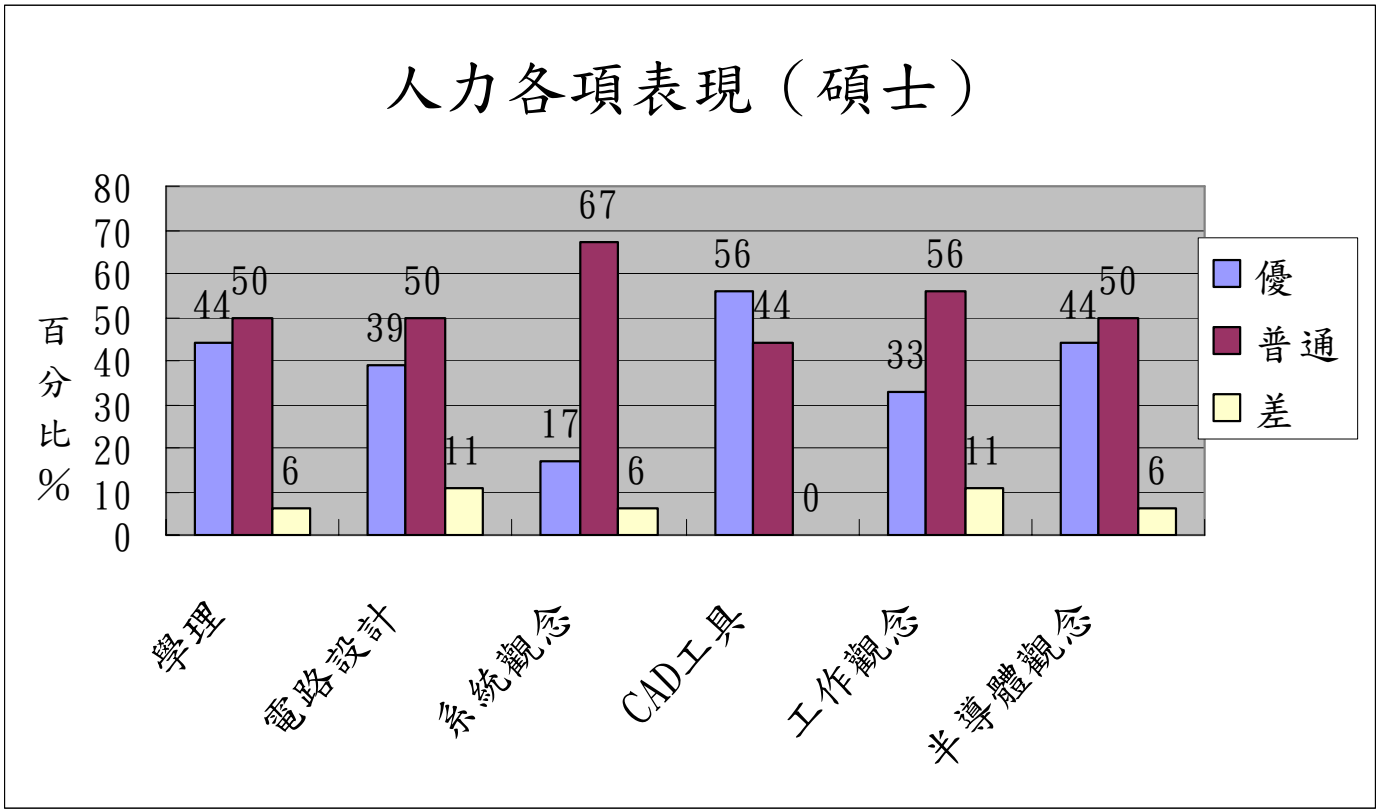
Part III

IC 設計業之人力

人力表現比較 (1)


工業界
各級人力各項表現（學士）
百分比
70
60
50
40
30
20
10
0
11
56
28
27
44
22
11
39
44
22
61
11
22
61
11
0
61
27
學理
電路設計
系統觀念
CAD工具
工作觀念
半導體觀念
優
普通
差

人力表現比較 (2)


人力各項表現（碩士）
百分比%
80
70
60
50
40
30
20
10
0
44
50
6
39
50
11
17
67
6
56
44
0
33
56
11
44
50
6
學理
電路設計
系統觀念
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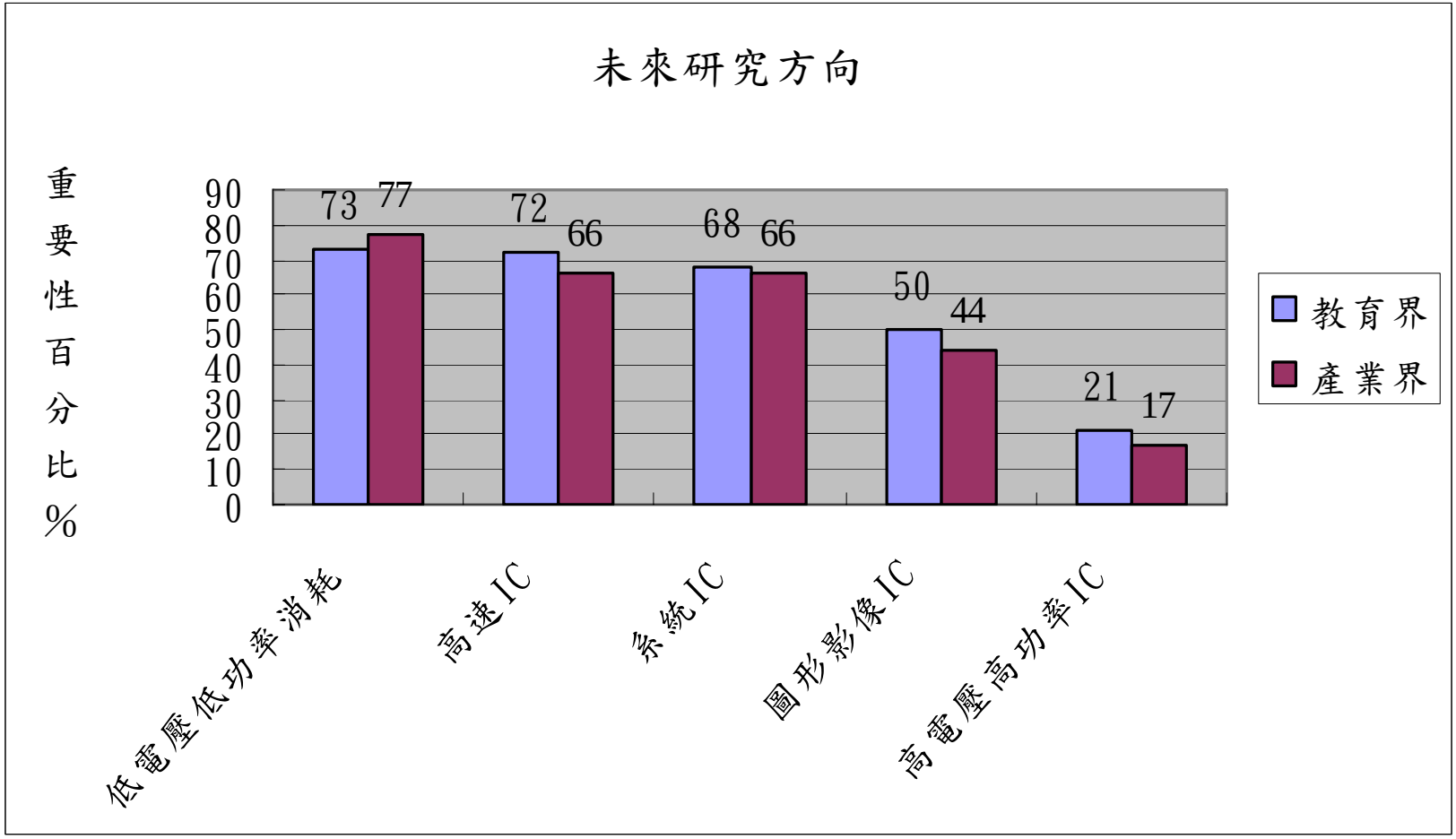
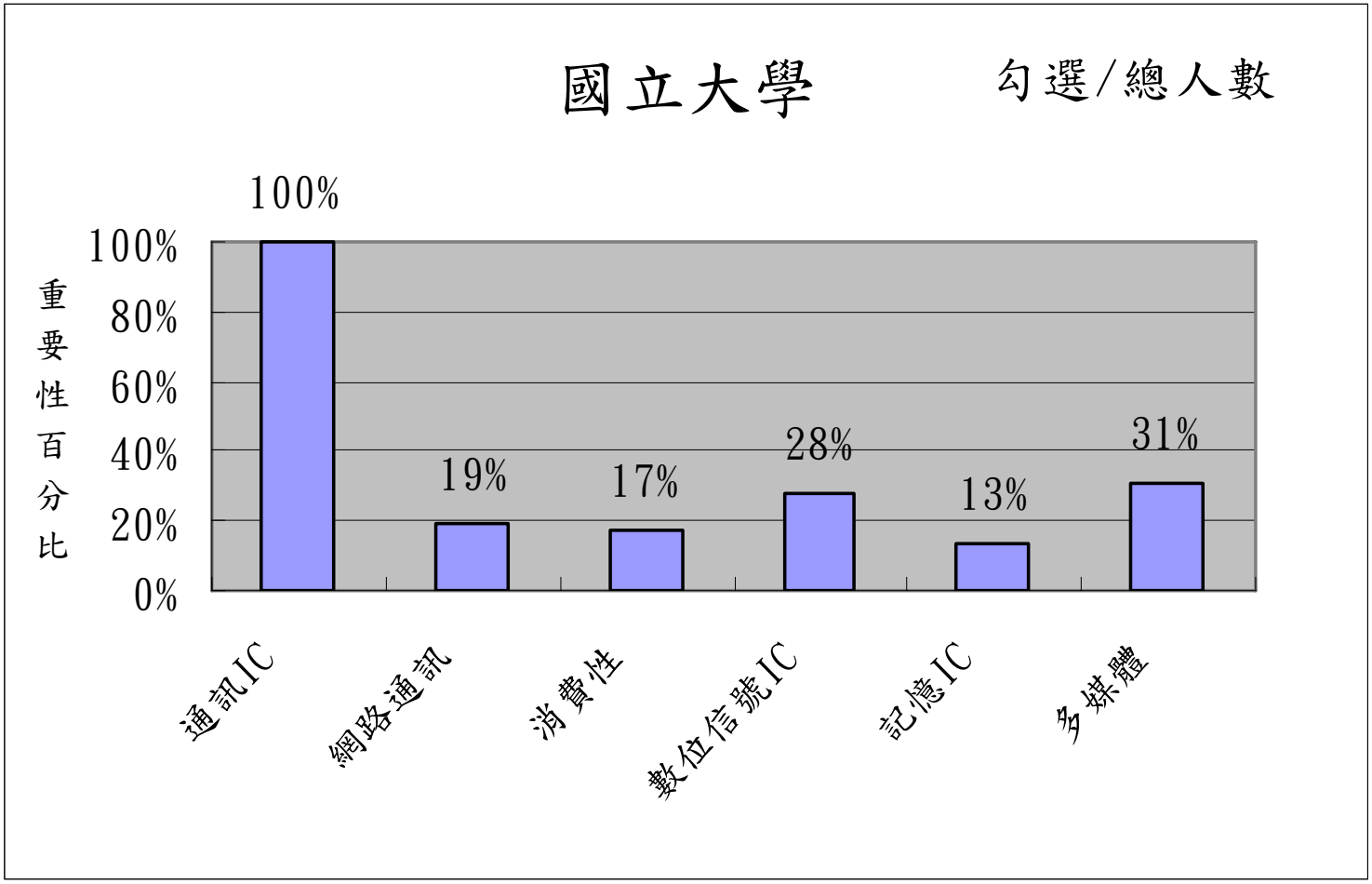
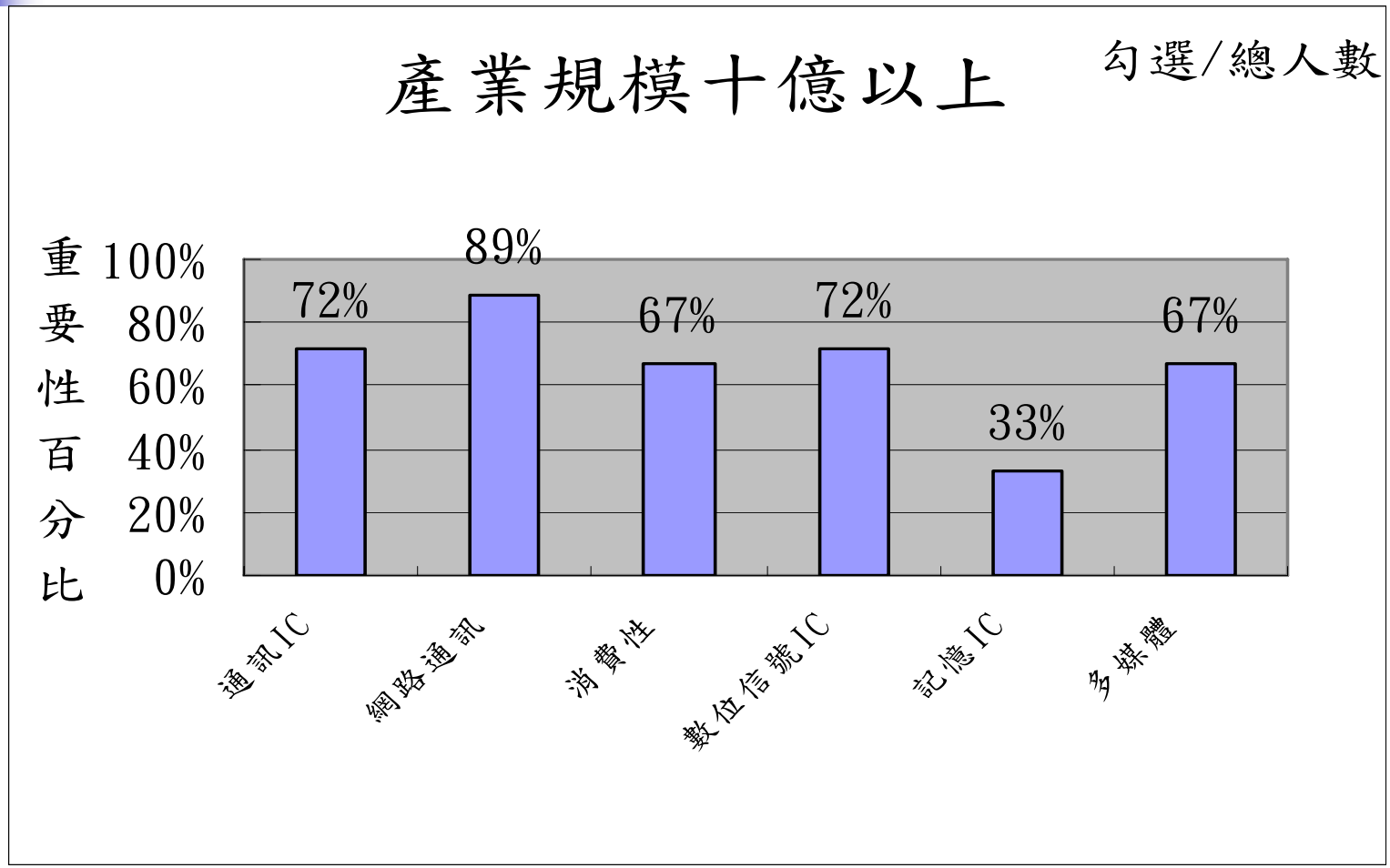
未來IC系統研究方向 (1)



未來IC系統研究方向 (2)



未來IC系統研究方向 (3)