From Thought to Realization : Innovative and Intelligent Hardware Architecture for Future Applications

Keep Exceeding : Past, Now, Future!

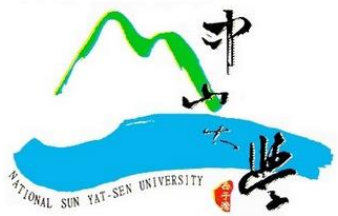
～ 用心就能讓彩虹收集好每一道顏色 ～

中山電機系 施信毓 教授

Outline

- Self Introduction
- Work I : Reconfigurable LEGO-based FFT Hardware
- Work II : Efficient LDPC Decoder with On-Line Customized-Matrix Downloading

Self Introduction



Self Introduction

年輕 活力 熱情 拚勁

總要為青春寫下新頁
總要為生命留下足跡

* 職稱 ：
  - 中山電機系 系統晶片組(SOC) 助理教授(2015/08~)
  - 圖資處 資訊安全組 組長(2018/02~)
* 經歷 ：
  - 圖資處 網路系統組 組長(2016/08~2018/01)
  - 聯發科技 資深工程師(2010/08~2014/11)
* 學歷 ：
  - 台大電子博士(2010)
  - 台大電子碩士(2006)
  - 清大電機學士(2004)
* 學術專長 ：
  - 通訊系統晶片設計
  - 數位電路設計
  - 數位訊號處理
  - 錯誤更正碼

■ 實驗室 ： 智慧型創新系統晶片設計實驗室(SNSD-IC LAB)

Academic Performance : Current

- 榮獲第七屆有庠科技發明獎
- 國際期刊論文發表 ： 共 4 篇
  - 第一等國際期刊論文發表 ： IEEE Transactions on Circuits and Systems I : Regular Papers (TCAS-I) 2篇
- 國際會議論文發表 ： 共 20 篇
- 指導學生論文榮獲 :「 2016 IEEE GCCE Student Paper Award (3rd Prize) 」
- 指導學生榮獲 :「 2017第十七屆旺宏金矽獎-設計組優勝獎 」
- 指導學生榮獲 :「 2016年全國大專院校智慧電子與資通應用創新創意競賽第一名 」(共118支隊伍參賽)
- 指導學生榮獲 :「 2017光電與通訊工程應用研討會最佳論文獎 」
- 通過“科技部新進教授計畫-2年期”
- 獲頒國立中山大學104學年度“新進教師獎勵“之殊榮
- 當選校內教學優良課程 ： 1061「系統晶片設計」

2015/08～迄今(持續增加中)

Academic Performance : Past

- IC設計領域之最頂尖國際期刊發表:Journal of Solid-State Circuits (JSSC)
- IC設計領域之最重要國際會議論文發表:IEEE Symposium on VLSI Circuits (SOVC)
- 甄選上2009 第一屆IEEE ISSCC Student Forum:全世界每年只遴選30名博士生
- 2005 ~ 2009 七座旺宏金矽獎:包含「最佳創意獎」和「評審團金獎」(當年首獎)
- 2007 & 2009 兩座國家晶片系統設計中心(CIC)「優良晶片設計獎」
- 95學年度大學院校積體電路設計競賽「標準單元設計組佳作」
- 2007第二屆鳳凰盃IC設計競賽「數位IC設計組優等獎」
- 94學年度台大電子所「最佳碩士論文獎」
- 2007台大電子所「學生傑出研究獎」
- 獲選為99年度台大「優秀青年」
- 獲選為救國團「全國大專優秀青年」
- 兩項中華民國和美國等專利:
  此專利技術轉移給國際廠商 (2013年)

Paper Citation Performance (Highlight)

- 高論文引用數：JSSC paper citation
  - 在10年間(2008~2018), 已累積達153次(持續增加中)

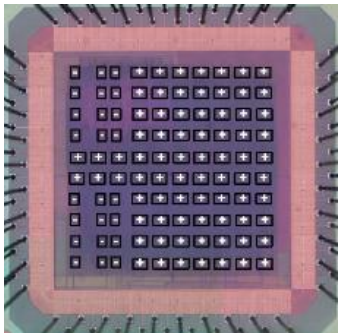
An 8.29 mm^2 52 mW Multi-Mode LDPC Decoder Design for Mobile WiMAX System in 0.13 μm CMOS Process

XY Shih, CZ Zhan, CH Lin... - IEEE Journal of Solid-State ..., 2008 - ieeexplore.ieee.org

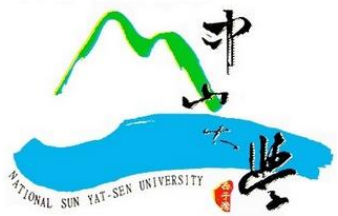
Abstract: This paper presents a multi-mode decoder design for Quasi-Cyclic LDPC codes for Mobile WiMAX system. This chip can be operated in 19 kinds of modes specified in Mobile WiMAX system, including block sizes of 576,..., 2304. There are four proposed design

☆ 99 被引用 153 次 相關文章 全部共 9 個版本 Web of Science: 81

- 研究主題：低密度奇偶校驗編碼之解碼器 (LDPC decoder)
- 重要貢獻：
  - 數學理論@1962年：目前通訊上最強大的錯誤更正碼
  - 最大挑戰：
    - 晶片面積大(成本大) & 消耗功率高
    - 支援多模式的解碼器

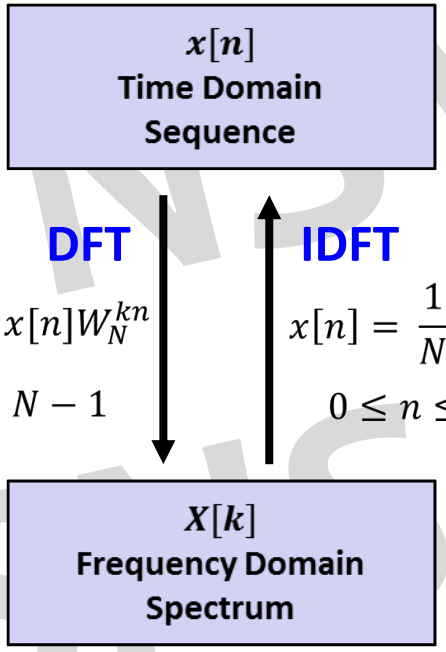


Work I : Reconfigurable LEGO-based FFT Hardware



Definition of DFT and FFT

- Discrete Fourier Transform (DFT) & Inverse DFT (IDFT)

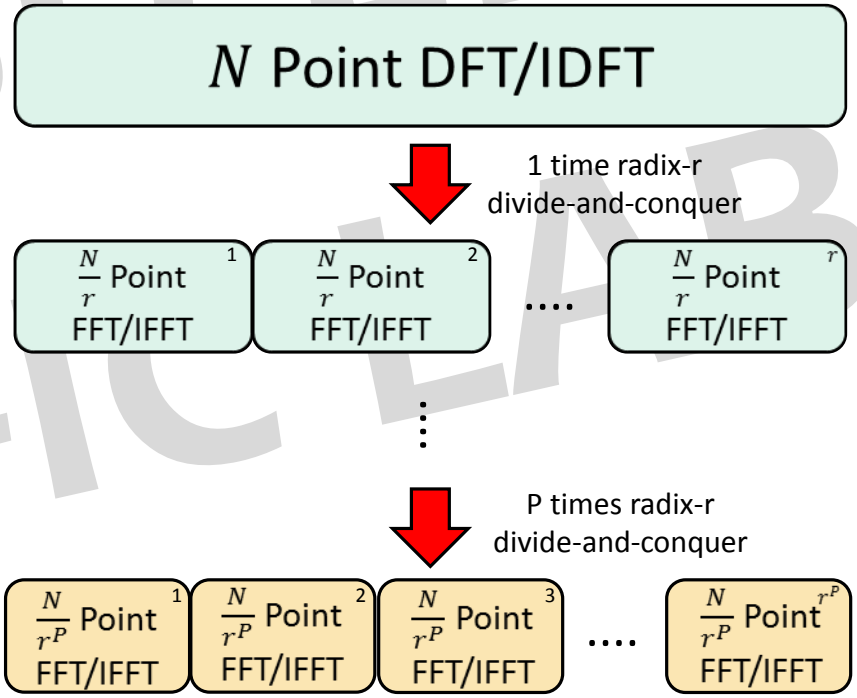


$$X[k] = \sum_{n=0}^{N-1} x[n] W_N^{kn} \qquad 0 \le k \le N-1$$

$$x[n] = \frac{1}{N} \sum_{n=0}^{N-1} X[k] W_N^{-kn} \qquad 0 \le n \le N-1$$

Twiddle Factor : $W_N = e^{-j\frac{2\pi}{N}}$

- Fast Fourier Transform (FFT) & Inverse FFT (IFFT)
  - Divide-and-Conquer

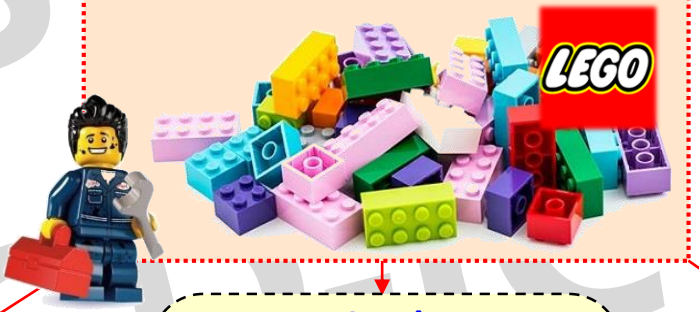


Concept of LEGO [1]

Vehicle

Camera

Hexacopter

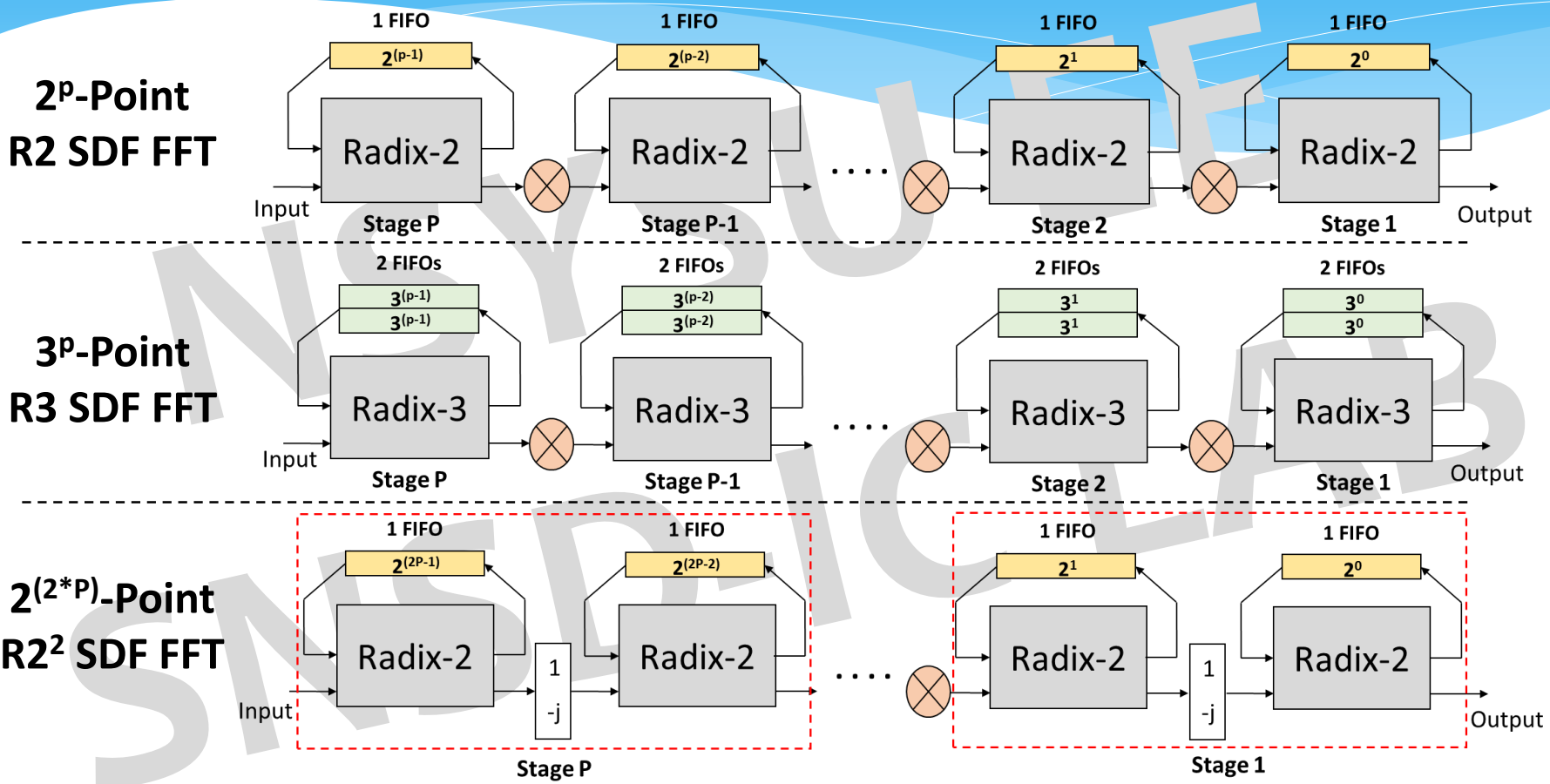


Food

Castle

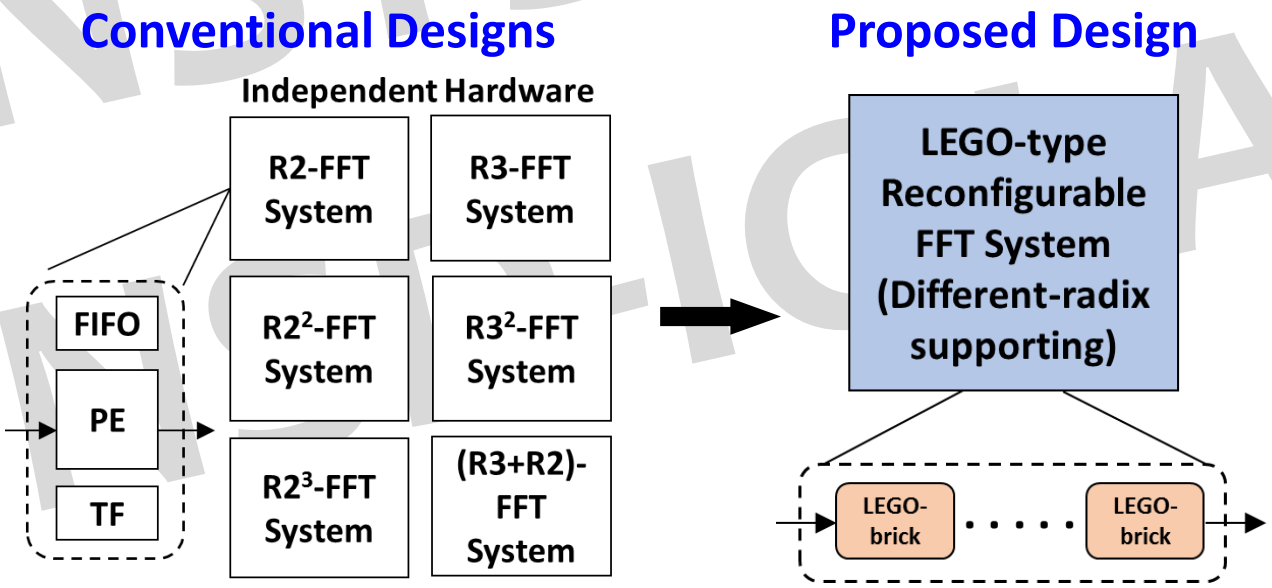
Kids' Toys

Single-Radix SDF FFT: R2, R3, & $R2^2$



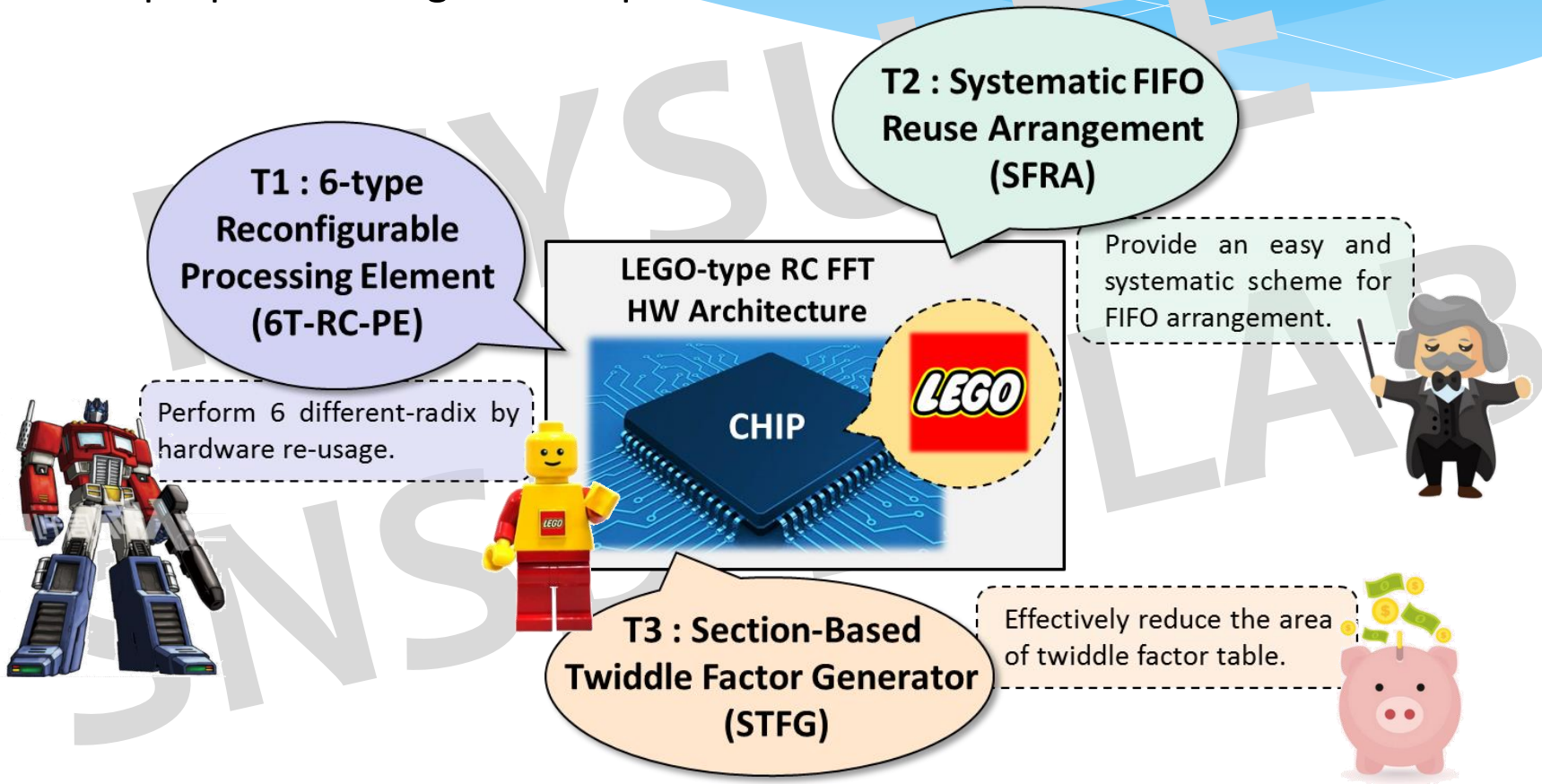
Reconfigurable LEGO-Based FFT Hardware

- Conventional SDF FFT needs extra hardware to support different-radix operation.
- We propose a **RC LEGO-based SDF FFT**, which is able to support different kinds of radix operations.



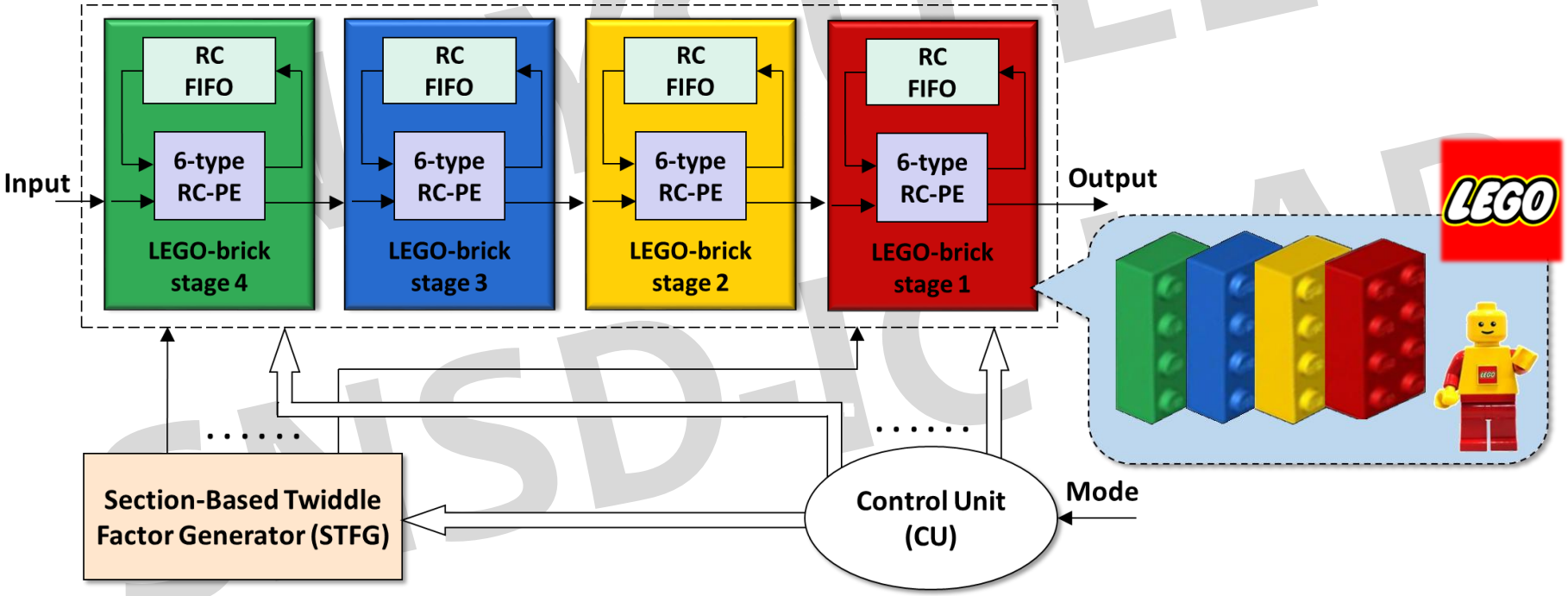
Proposed Design Techniques

- We propose 3 design techniques as follows :



Proposed System Architecture

- Each LEGO-brick contains RC FIFO (SFRA) and 6-type RC-PE.



48-Mode Configuration

- There are totally 48 different modes, depending on the valid (a, b) combinations which support 32 operating modes defined in 3GPP-LTE standard.

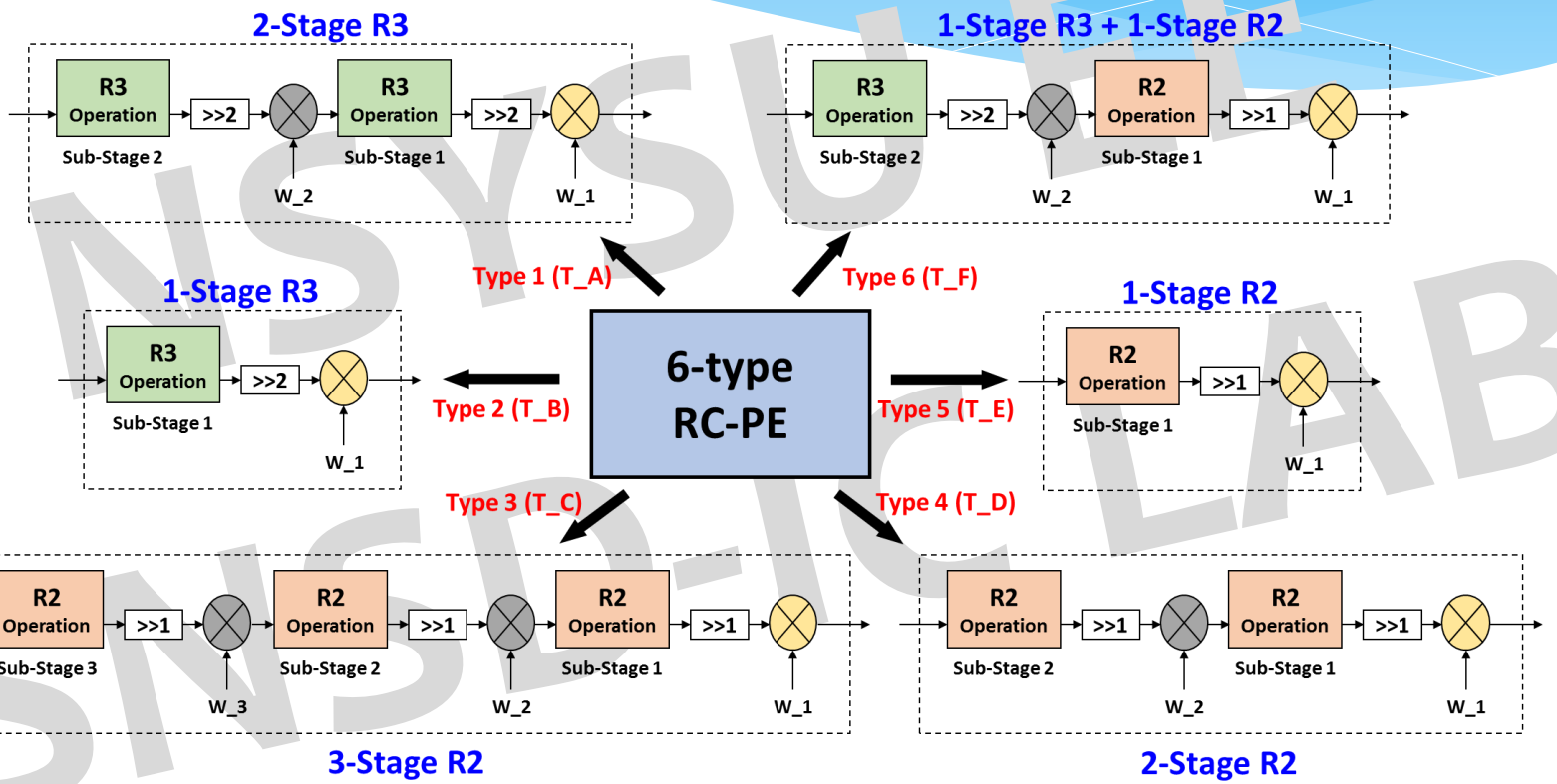
Category	FFT Profile	Possible Combination Set Based on Radix-3^2 and Radix-2^3 Bases										# of FFT Size
1	(a, b)	(7,0)										1
	FFT Point	2187										
2	(a, b)	(6,1)	(6,0)									2
	FFT Point	1458	729									
3	(a, b)	(5,3)	(5,2)	(5,1)	(5,0)							4
	FFT Point	1944	972	486	243							
4	(a, b)	(4,4)	(4,3)	(4,2)	(4,1)	(4,0)						5
	FFT Point	1296	648	324	162	81						
5	(a, b)	(3,6)	(3,5)	(3,4)	(3,3)	(3,2)	(3,1)	(3,0)				7
	FFT Point	1728	864	432	216	108	54	27				
6	(a, b)	(2,7)	(2,6)	(2,5)	(2,4)	(2,3)	(2,2)	(2,1)	(2,0)			8
	FFT Point	1152	576	288	144	72	36	18	9			
7	(a, b)	(1,9)	(1,8)	(1,7)	(1,6)	(1,5)	(1,4)	(1,3)	(1,2)	(1,1)	(1,0)	10
	FFT Point	1536	768	384	192	96	48	24	12	6	3	
8	(a, b)	(0,11)	(0,10)	(0,9)	(0,8)	(0,7)	(0,6)	(0,5)	(0,4)	(0,3)	(0,2)	(0,1)	11
	FFT Point	2048	1024	512	256	128	64	32	16	8	4	2	
												Total	48

(a, b) represents $3^a * 2^b$- FFT point

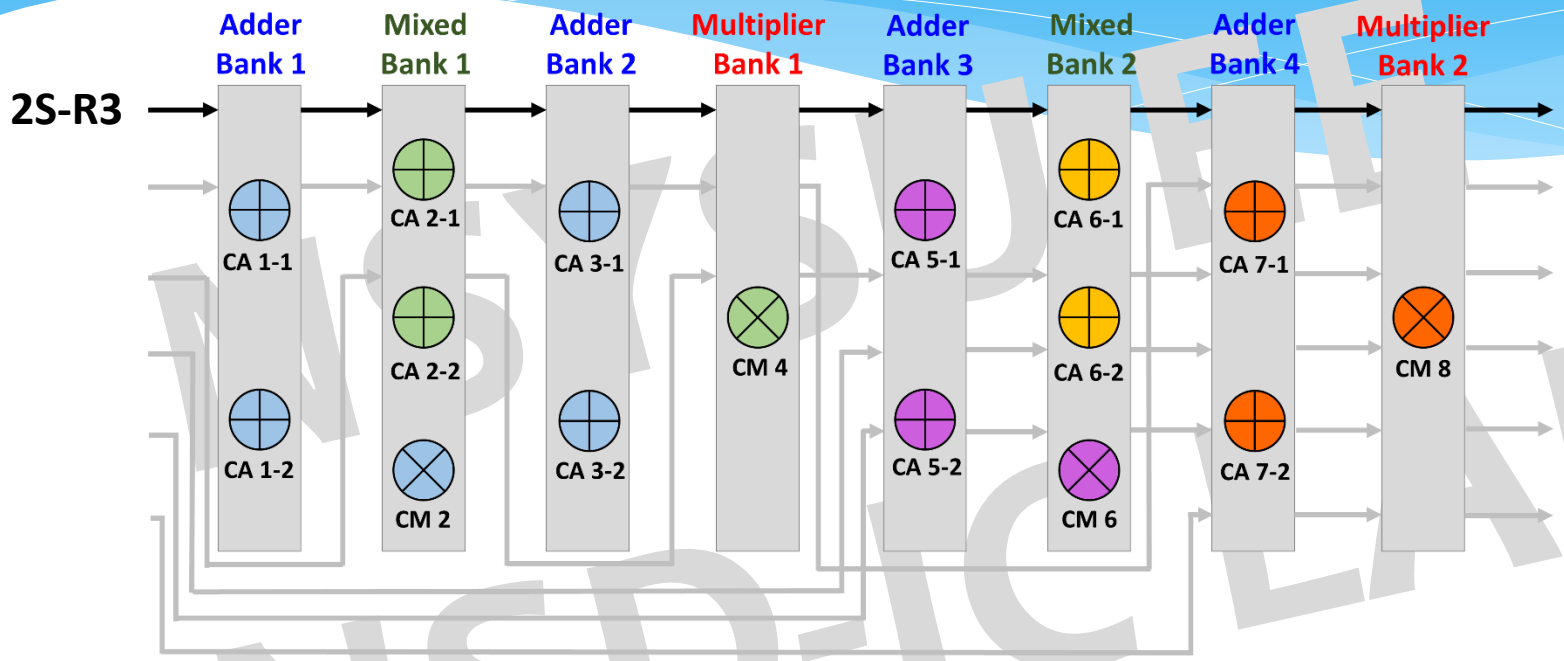
Note : ▭ indicates the FFT points defined in 3GPP-LTE standard .

T1 : 6T-RC-PE : Design Concept

- Our proposed 6-type RC PE has 6 different-radix operating types.



T1 : 6T-RC-PE : 2S-R3 (T_A)



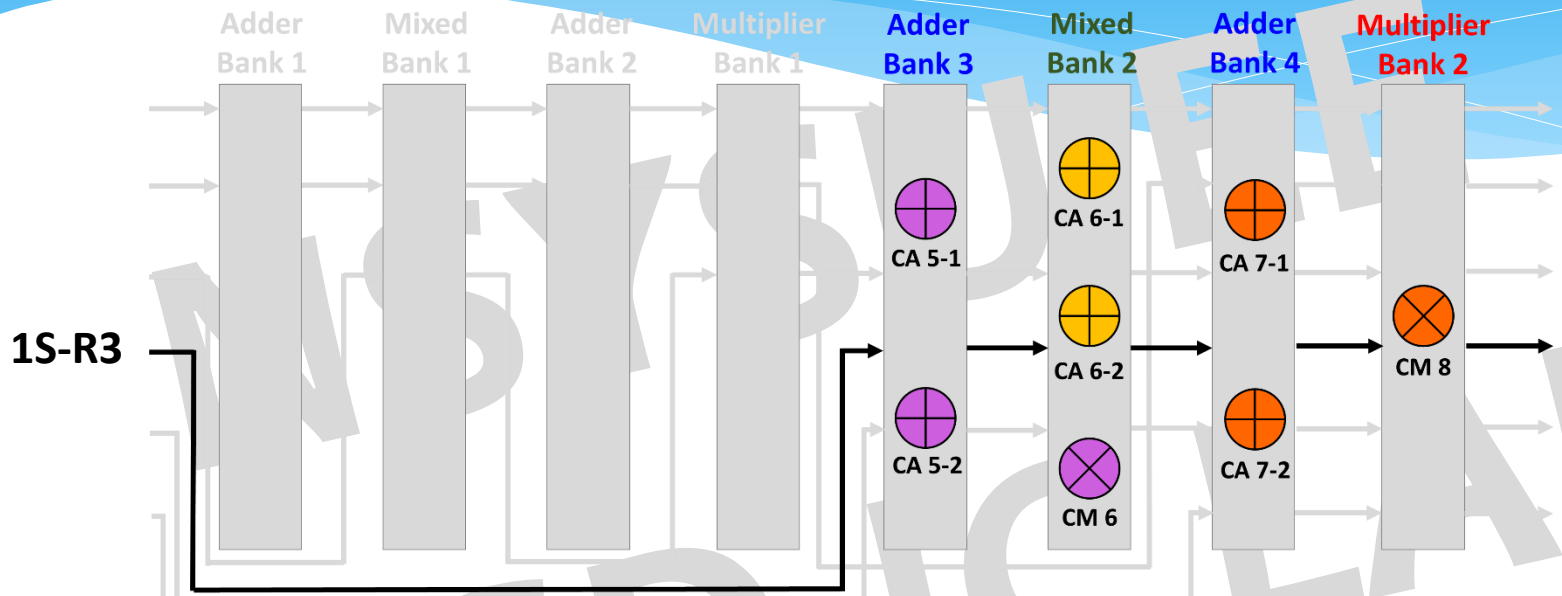
aS-R3 : a-Stage of Radix-3 (a=1, 2)
bS-R2 : b-Stage of Radix-2 (b=1, 2, 3)
R3-R2 : 1-Stage of Radix-3 concatenated with 1-Stage of Radix-2

: All modes
: 2S-R3 & 1S-R3 modes
: 2S-R3 & R3-R2 modes
: 2S-R3, R3-R2 & 3S-R2 modes
: 2S-R3, 1S-R3, 3S-R2 & 2S-R2 modes

CA : Complex Adder
CM : Complex Multiplier

Hardware Resource
CA : 12/12 (100.0%)
CM : 4/4 (100.0%)

T1 : 6T-RC-PE : 1S-R3 (T_B)



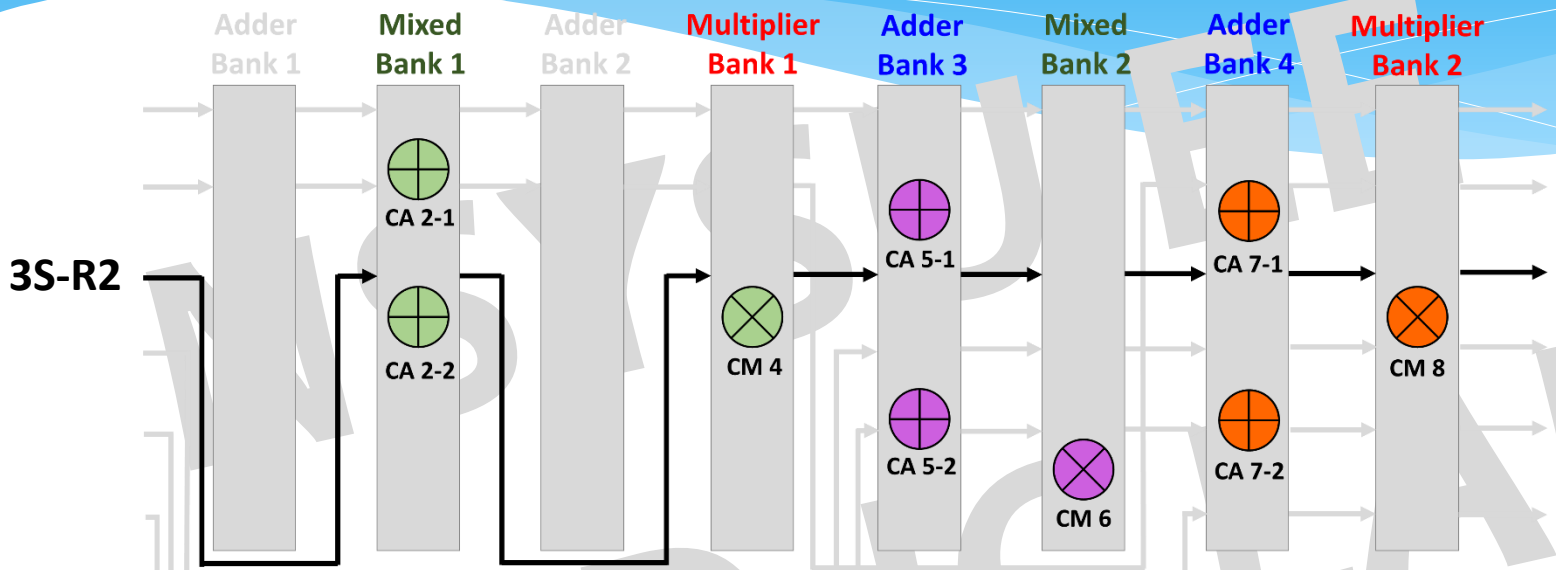
aS-R3 : a-Stage of Radix-3 (a=1, 2)
bS-R2 : b-Stage of Radix-2 (b=1, 2, 3)
R3-R2 : 1-Stage of Radix-3 concatenated with 1-Stage of Radix-2

: All modes
: 2S-R3 & 1S-R3 modes
: 2S-R3 & R3-R2 modes
: 2S-R3, R3-R2 & 3S-R2 modes
: 2S-R3, 1S-R3, 3S-R2 & 2S-R2 modes

CA : Complex Adder
CM : Complex Multiplier

Hardware Resource
CA : 6/12 (50.0%)
CM : 2/4 (50.0%)

T1 : 6T-RC-PE : 3S-R2 (T_C)



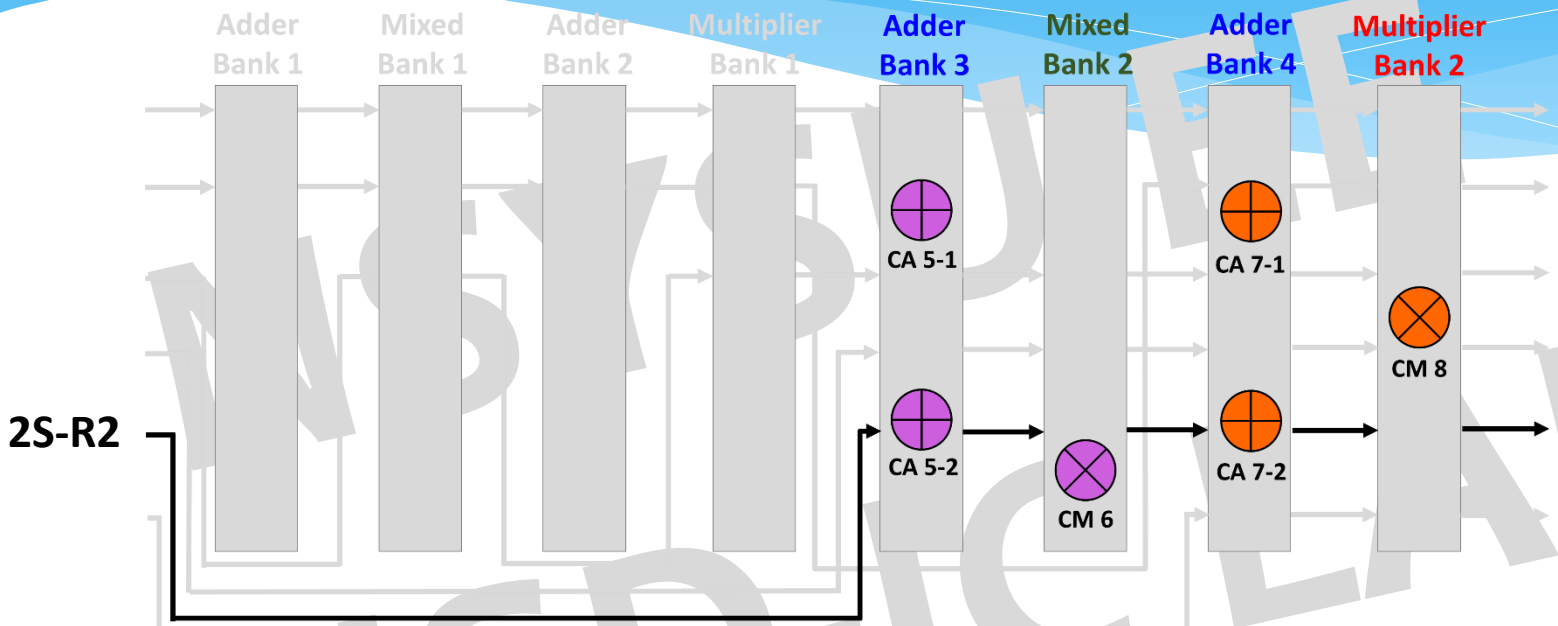
aS-R3 : a-Stage of Radix-3 (a=1, 2)
bS-R2 : b-Stage of Radix-2 (b=1, 2, 3)
R3-R2 : 1-Stage of Radix-3 concatenated with 1-Stage of Radix-2

: All modes
: 2S-R3 & 1S-R3 modes
: 2S-R3 & R3-R2 modes
: 2S-R3, R3-R2 & 3S-R2 modes
: 2S-R3, 1S-R3, 3S-R2 & 2S-R2 modes

CA : Complex Adder
CM : Complex Multiplier

Hardware Resource
CA : 6/12 (50.0%)
CM : 3/4 (75.0%)

T1 : 6T-RC-PE : 2S-R2 (T_D)



aS-R3 : a-Stage of Radix-3 (a=1, 2)
bS-R2 : b-Stage of Radix-2 (b=1, 2, 3)
R3-R2 : 1-Stage of Radix-3 concatenated with 1-Stage of Radix-2

: All modes
: 2S-R3 & 1S-R3 modes
: 2S-R3 & R3-R2 modes
: 2S-R3, R3-R2 & 3S-R2 modes
: 2S-R3, 1S-R3, 3S-R2 & 2S-R2 modes

CA : Complex Adder
CM : Complex Multiplier

Hardware Resource
CA : 4/12 (33.3%)
CM : 2/4 (50.0%)

T1 : 6T-RC-PE : 1S-R2 (T_E)

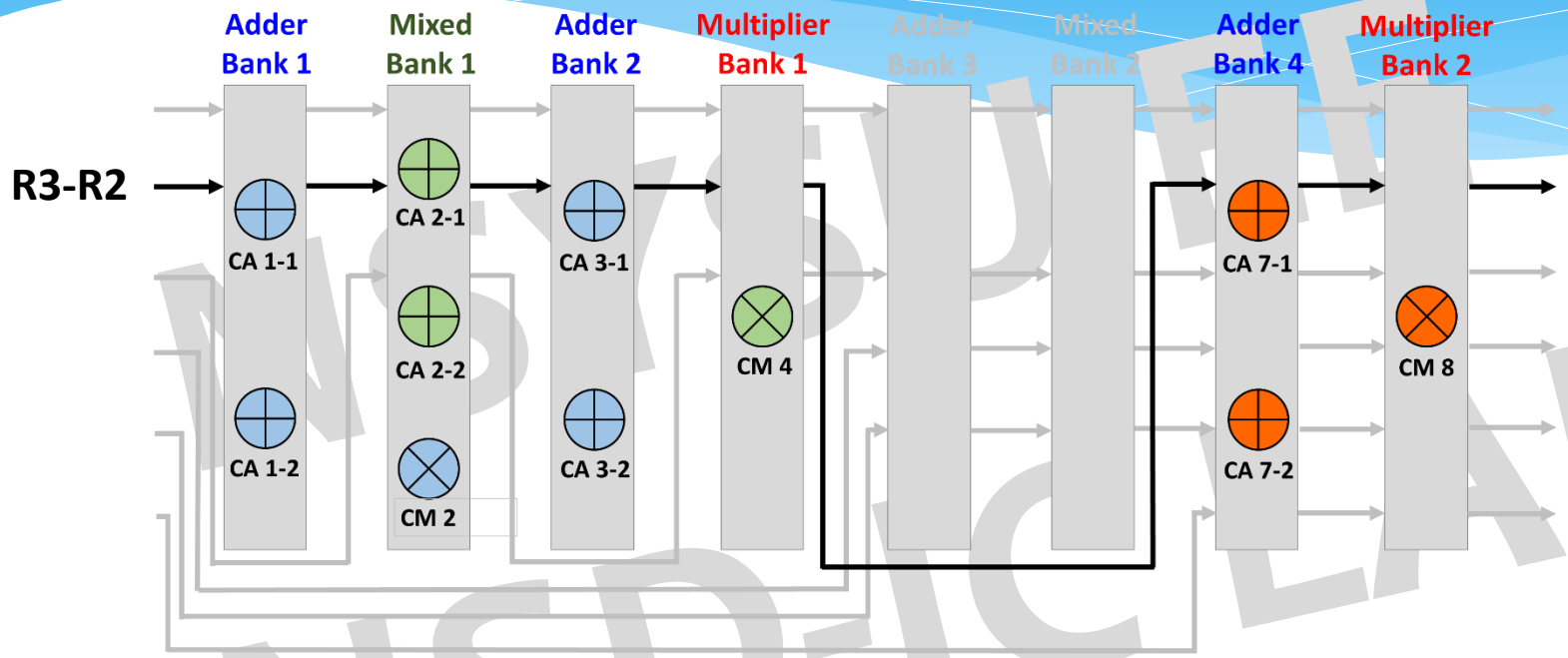
aS-R3 : a-Stage of Radix-3 (a=1, 2)
bS-R2 : b-Stage of Radix-2 (b=1, 2, 3)
R3-R2 : 1-Stage of Radix-3 concatenated with 1-Stage of Radix-2

: All modes
: 2S-R3 & 1S-R3 modes
: 2S-R3 & R3-R2 modes
: 2S-R3, R3-R2 & 3S-R2 modes
: 2S-R3, 1S-R3, 3S-R2 & 2S-R2 modes

CA : Complex Adder
CM : Complex Multiplier

Hardware Resource
CA : 2/12 (16.7%)
CM : 1/4 (25.0%)

T1 : 6T-RC-PE : R3-R2 (T_F)



aS-R3 : a-Stage of Radix-3 (a=1, 2)
bS-R2 : b-Stage of Radix-2 (b=1, 2, 3)
R3-R2 : 1-Stage of Radix-3 concatenated with 1-Stage of Radix-2

: All modes
: 2S-R3 & 1S-R3 modes
: 2S-R3 & R3-R2 modes
: 2S-R3, R3-R2 & 3S-R2 modes
: 2S-R3, 1S-R3, 3S-R2 & 2S-R2 modes

CA : Complex Adder
CM : Complex Multiplier

Hardware Resource
CA : 8/12 (66.7%)
CM : 3/4 (75.0%)

6T-RC-PE : Synthesis Results

TSMC 40-nm

- Our proposed 6T-RC-PE reduces the computing unit effectively.

	Hardware Resource					Cost Saving	
	Traditional Single-Radix FFT PE				6T-RC-PE (R)		
	2S-R3 (M1)	3S-R2 (M2)	R3-R2 (M3)	Total (M) (Sum(Mi))		Value (M-R)	Ratio (M-R)/M
CA	12	6	8	26	12	14	53.8%
CM	9	2	5	16	4	12	75.0%

- As wordlength changes from 12 to 18, the cost saving ratios are 64.5% to 67.7%.

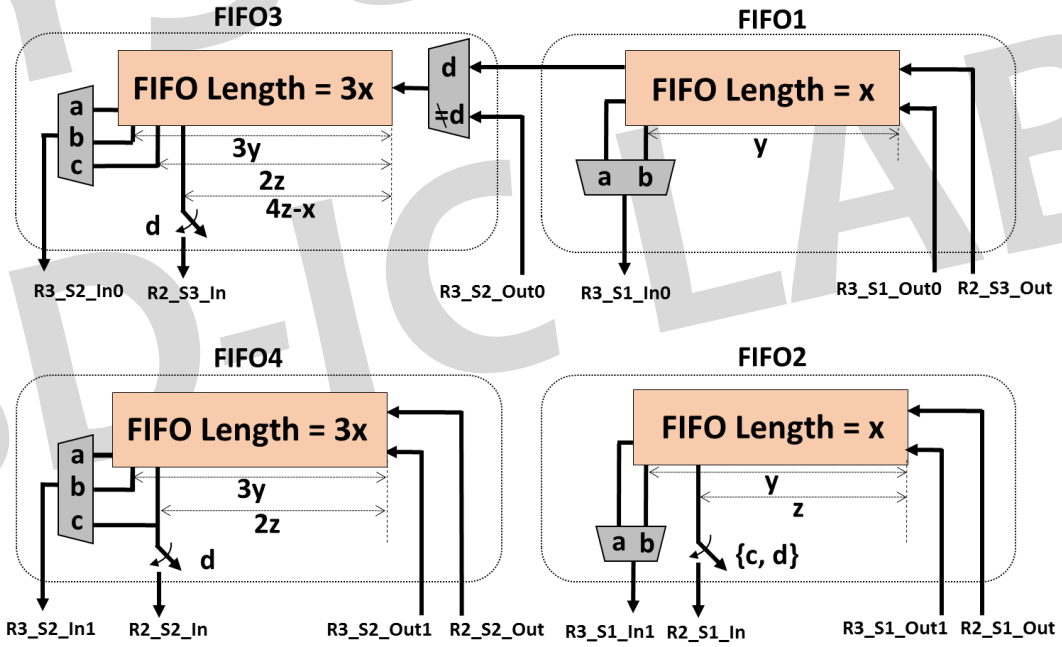
Wordlength (Bits)	Hardware Resource					Cost Saving	
	Traditional Single-Radix FFT PE				6T-RC-PE (R)		
	2S-R3 (M1)	3S-R2 (M2)	R3-R2 (M3)	Total (M) (Sum(Mi))		Value (M-R)	Ratio (M-R)/M
12	22445.9	6403.2	12987.9	41837.0	14840.7	26996.3	64.5%
14	29376.5	8192.5	16927.4	54496.4	18782.1	35714.3	65.5%
16	37354.9	10201.0	21446.2	69002.1	22771.2	46230.9	67.0%
18	45212.6	12253.6	27915.3	85381.5	27612.0	57769.5	67.7%

PE : Processing Element CA : Complex Adder CM : Complex Multiplier

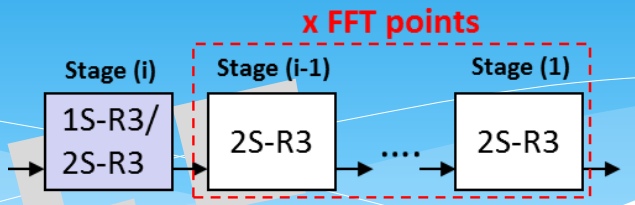
T2 : SFRA : Design Concept

- According to mode configuration, FIFOs are divided into 4 different conditions (a, b, c, d).
- Each LEGO-brick has a total FIFO length of 8x (3x+3x+x+x), where $x = 3^{2(i-1)}$ (i = 1-4).

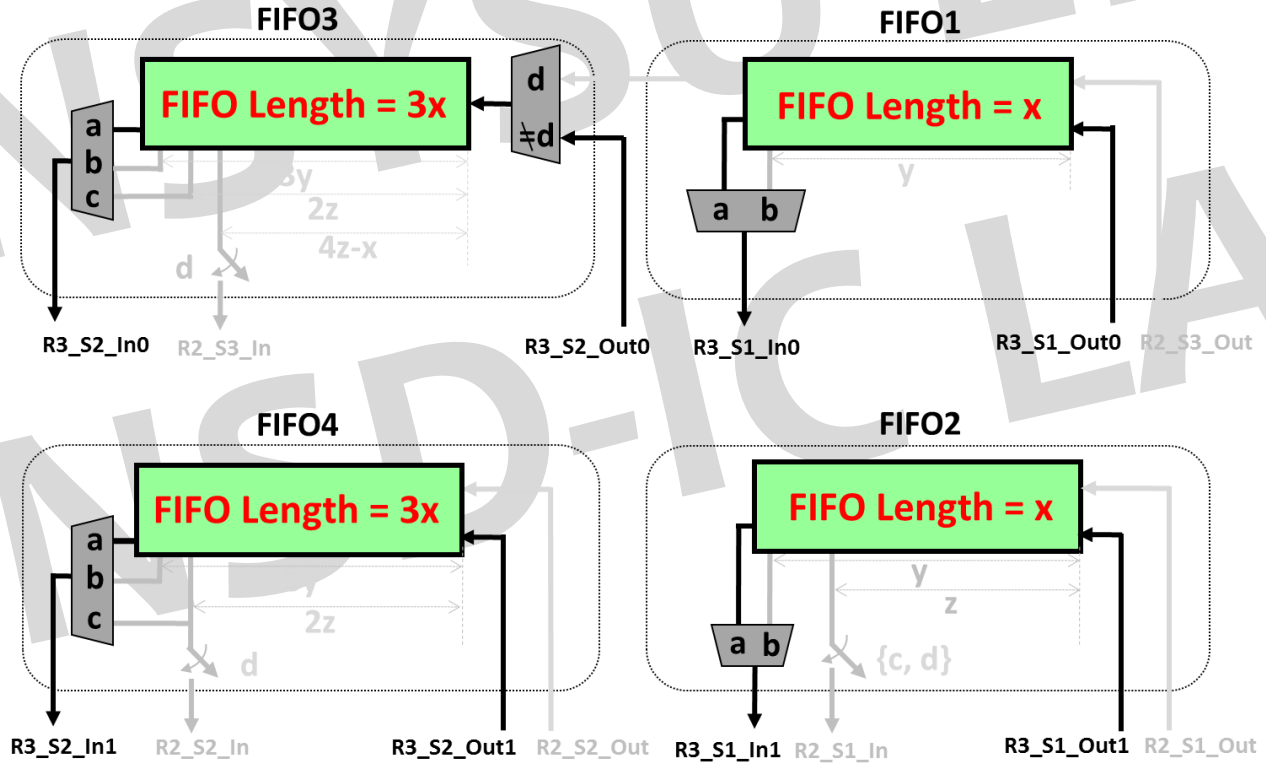
LEGO-brick stage (i)	FIFO Length Parameter (x)
1	1
2	9
3	81
4	729



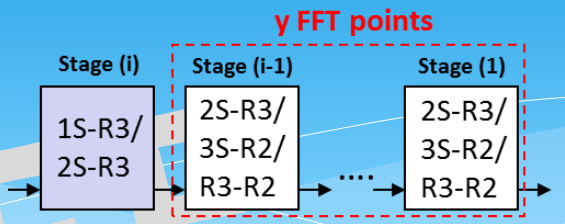
T2 : SFRA : Condition a



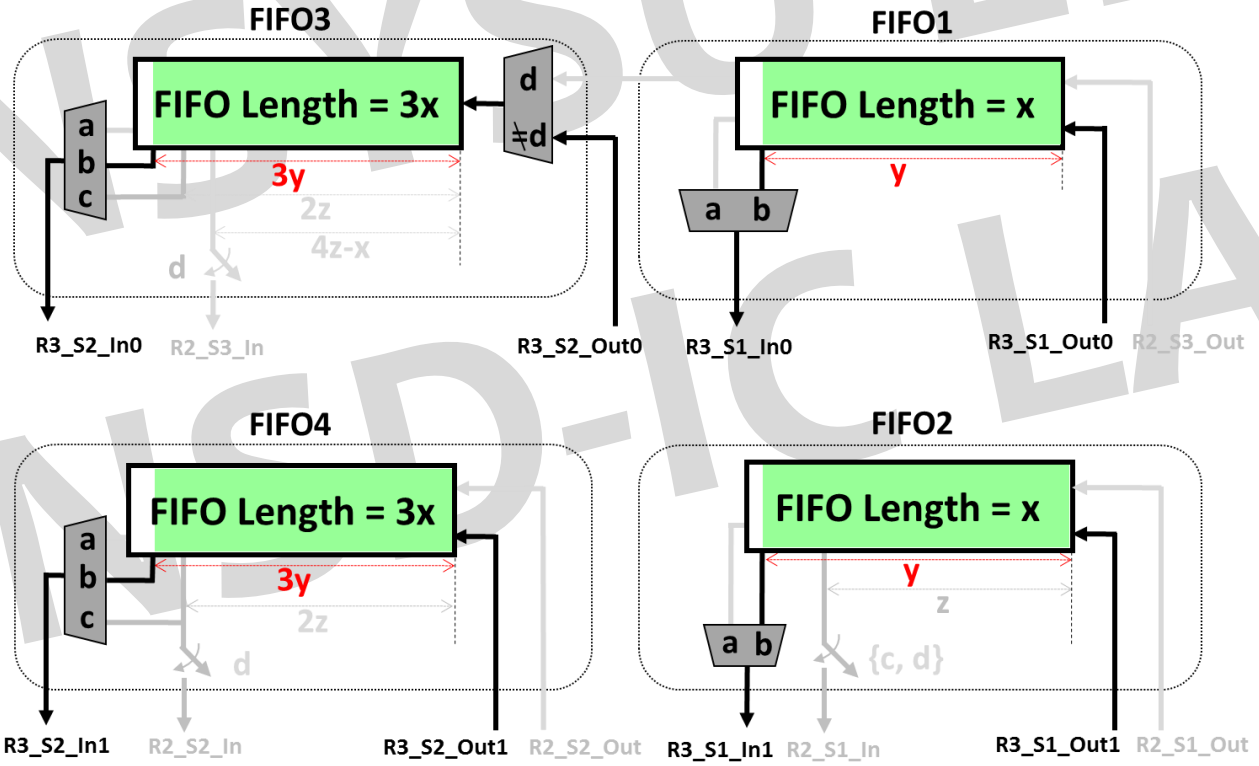
- Condition a :
  - Stage (i) is used to operate 1S-R3 & 2S-R3.
  - Stage (i-1) - Stage (1) perform x FFT points entirely, served as all 2S-R3.



T2 : SFRA : Condition b

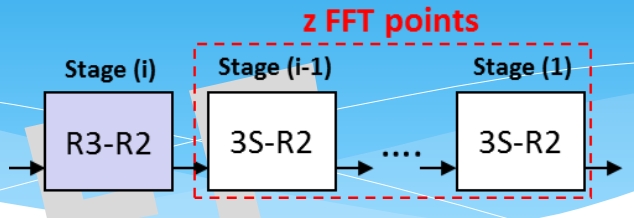


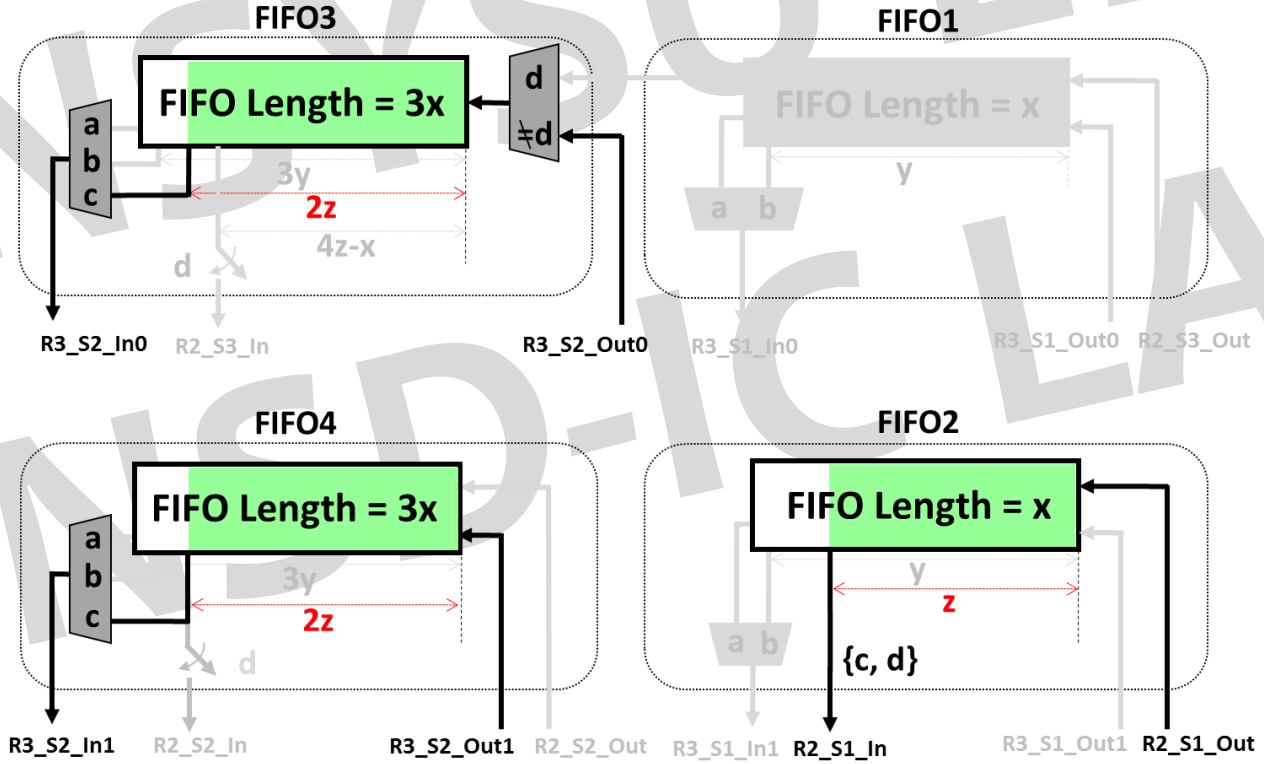
- Condition b :
  - Stage (i) is used to operate 1S-R3 & 2S-R3.
  - Stage (i-1) - Stage (1) perform y FFT points entirely, served as beyond all 2S-R3.



T2 : SFRA : Condition c

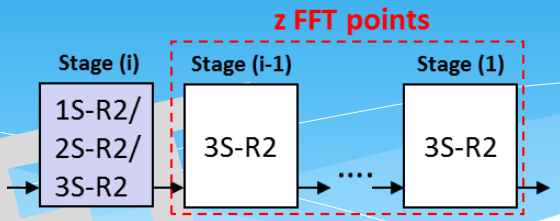
- Condition c :
  - Stage (i) is used to operate R3-R2.
  - Stage (i-1) - Stage (1) perform z FFT points entirely, served as all 3S-R2.

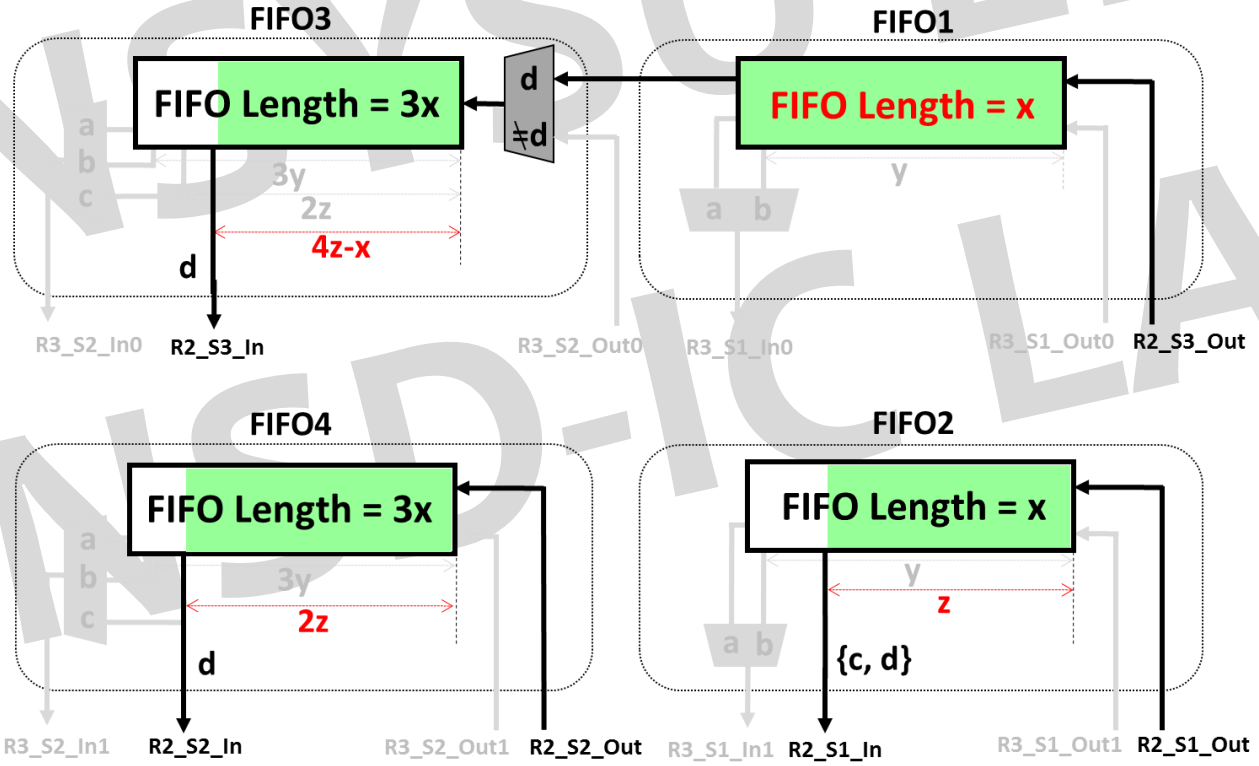




T2 : SFRA : Condition d

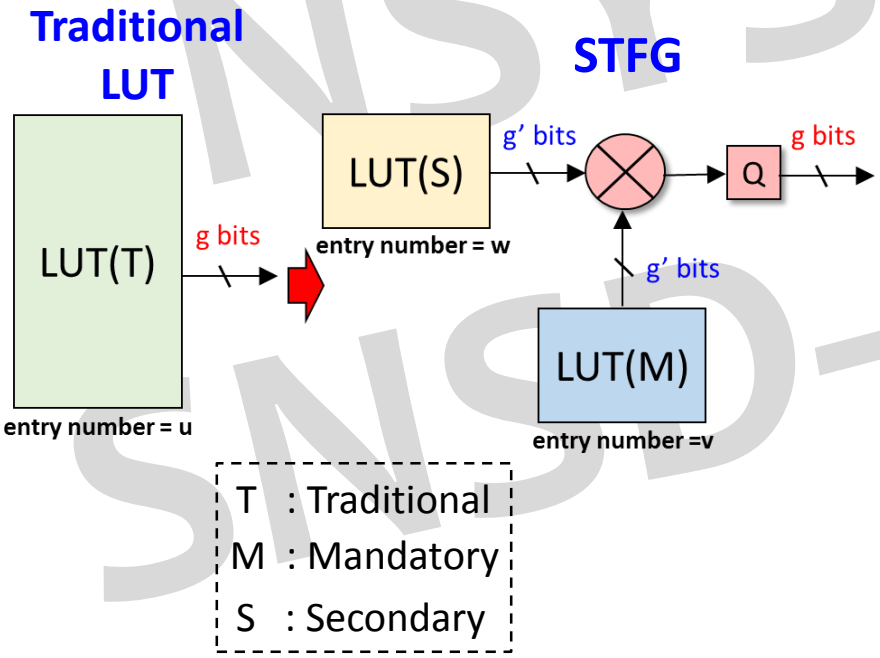
- Condition d :
  - Stage (i) is used to operate 1S-R2, 2S-R2, & 3S-R2.
  - Stage (i-1) - Stage (1) perform z FFT points entirely, served as all 3S-R2.

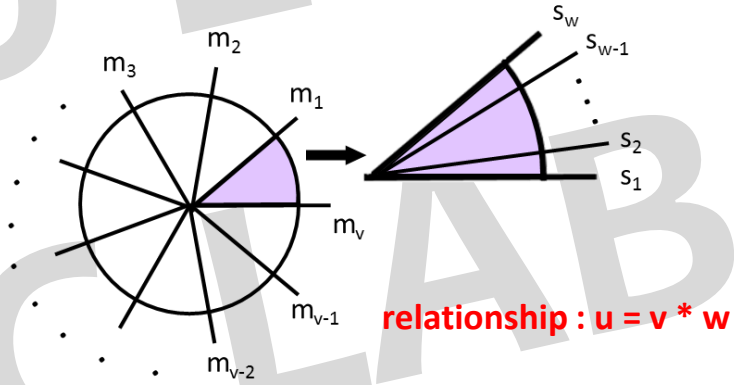




T3 : STFG : Design Concept

- Traditional LUT : Use the direct look-up table(LUT) to generate twiddle factor.
- Our proposed STFG : We use 2 smaller LUTs and one complex multiplier to implement the traditional LUT.





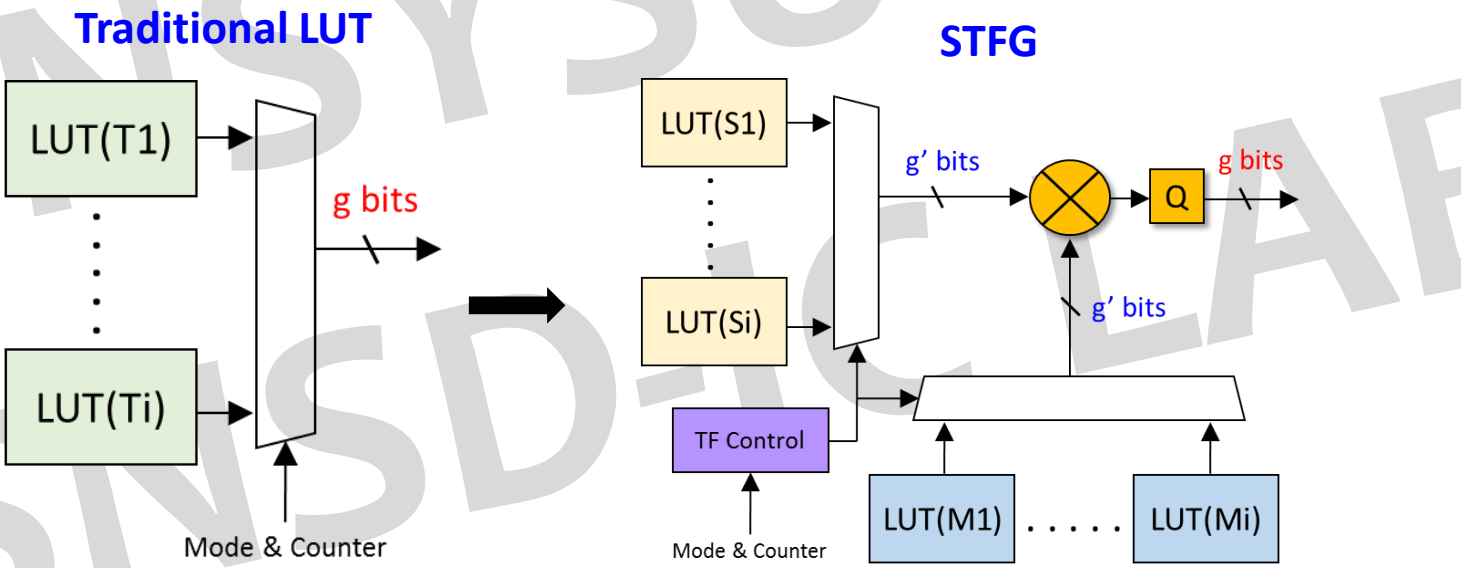
(1) W_u^k ,where k ={0,1,…,u-1}

(2) $W_u^k = W_v^{k1} \times W_{v*w}^{k2}$

,where k ={0,1,…,u-1}
k1={0,1,…,v-1}
k2={0,1,…,w-1}

T3 : STFG : Hardware Circuit

- STFG can be applied on LEGO-brick stage 3 and 4.
  - In LEGO-brick stage 3, it requires 10 kinds of table-modes(i=10).
  - In LEGO-brick stage 4, it requires 11 kinds of table-modes(i=11).



T : Traditional M : Mandatory S : Secondary

STFG : Synthesis Results

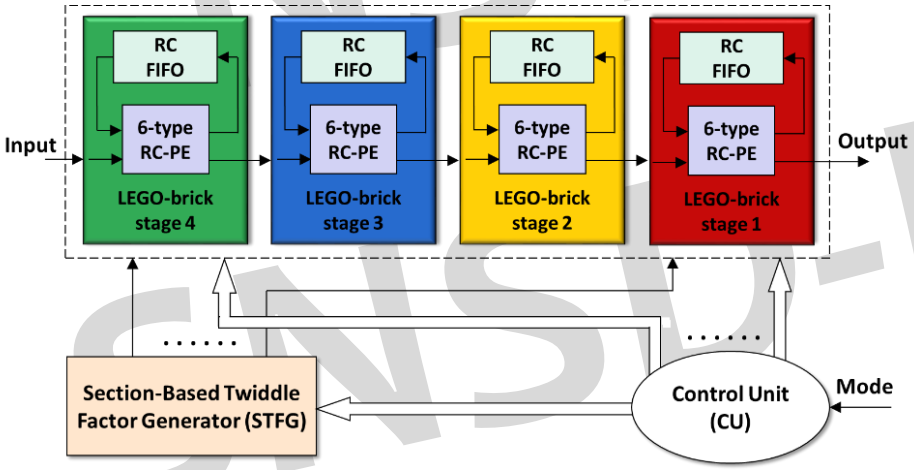
TSMC 40-nm

- As g' bits change from 16 to 8, the area saving ratios are shown in following table :
  - LEGO-brick stage 3 is from 20.0% to 60.4%.
  - LEGO-brick stage 4 is from 73.6% to 88.8%.

Circuit	g (bit)	g' (bit)	Traditional LUT Area (um^2) (T)	Section-Based Twiddle Factor Generator Area (um^2)					Area Saving	
				LUT (M) (R1)	LUT (S) (R2)	Multiplier (R3)	TF Control (R4)	Total (R) (sum (R_i))	Value (um^2) (T-R)	Reduced Ratio
LEGO-brick stage 3	16	8	9584.3	434.3 (11.4%)	533.3 (14.0%)	1019.7 (26.8%)	1811.7 (47.8%)	3798.9	5785.4	60.4%
		10		490.0 (10.6%)	601.7 (13.0%)	1568.2 (33.9%)	1961.4 (42.5%)	4621.3	4963.0	51.8%
		12		645.0 (11.6%)	792.0 (14.2%)	2170.0 (39.0%)	1959.1 (35.2%)	5566.1	4018.2	41.9%
		14		754.2 (11.5%)	926.2 (14.2%)	2902.3 (44.3%)	1959.6 (30.0%)	6542.3	3042.0	31.7%
		16		869.7 (11.3%)	1067.9 (13.9%)	3771.0 (49.2%)	1960.9 (25.6%)	7669.5	1914.8	20.0%
LEGO-brick stage 4	16	8	26217.2	411.7 (14.1%)	671.0 (22.9%)	1019.7 (34.8%)	824.9 (28.2%)	2927.3	23289.9	88.8%
		10		531.9 (14.0%)	867.1 (22.8%)	1568.2 (41.1%)	841.9 (22.1%)	3809.1	22408.1	85.5%
		12		647.5 (13.7%)	1055.5 (22.4%)	2170.3 (46.0%)	841.9 (17.9%)	4715.2	21502.0	82.0%
		14		759.0 (13.2%)	1237.1 (21.6%)	2891.7 (50.5%)	843.0 (14.7%)	5730.8	20486.4	78.1%
		16		875.4 (12.7%)	1426.9 (20.7%)	3758.8 (54.3%)	847.2 (12.3%)	6908.3	19308.9	73.6%

Synthesis Results : Proposed System

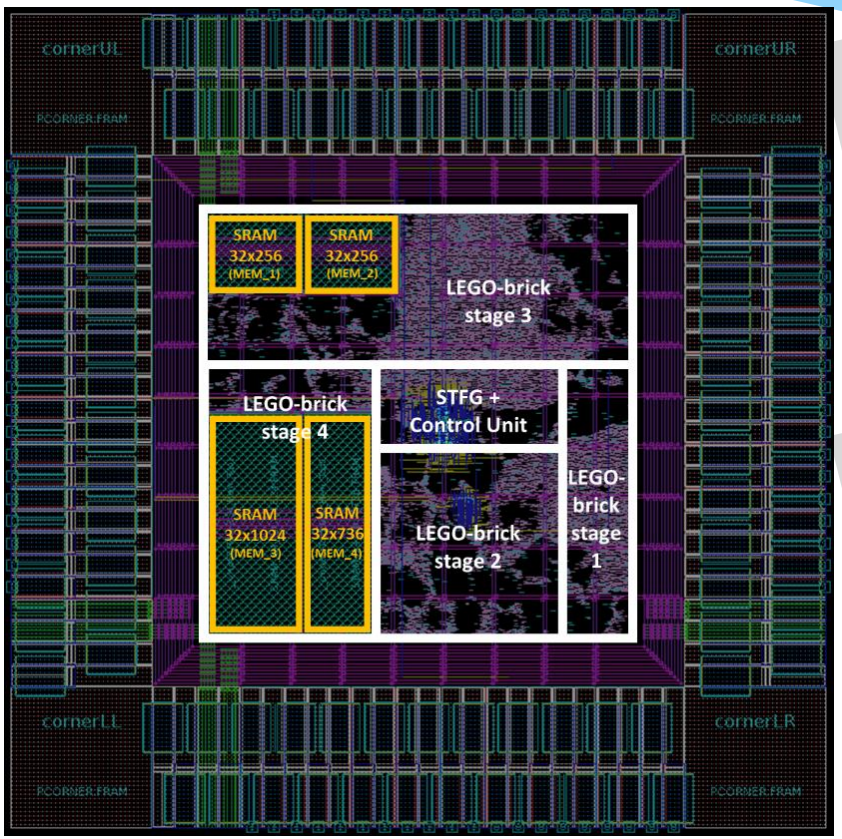
- In the TSMC 40-nm CMOS technology
  - Wordlength = 16 bits
  - Clock Frequency = 400MHz
  - Overall Circuit Area = 0.2367mm^2



Sub-circuits		Synthesis Area (mm^2)		
		Value	Ratio	
LEGO-brick stage 1	RC-FIFO	0.0020	0.9%	9.2%
	6T-RC-PE	0.0198	8.3%	
LEGO-brick stage 2	RC-FIFO	0.0150	6.3%	16.2%
	6T-RC-PE	0.0235	9.9%	
LEGO-brick stage 3	RC-FIFO	0.0590	24.9%	34.8%
	6T-RC-PE	0.0235	9.9%	
LEGO-brick stage 4	RC-FIFO	0.0645	27.4%	32.8%
	6T-RC-PE	0.0127	5.4%	
STFG		0.0115	4.8%	7.0%
Control Unit (CU)		0.0052	2.2%	
Total		0.2367	100.0%	100.0%

Chip Summary

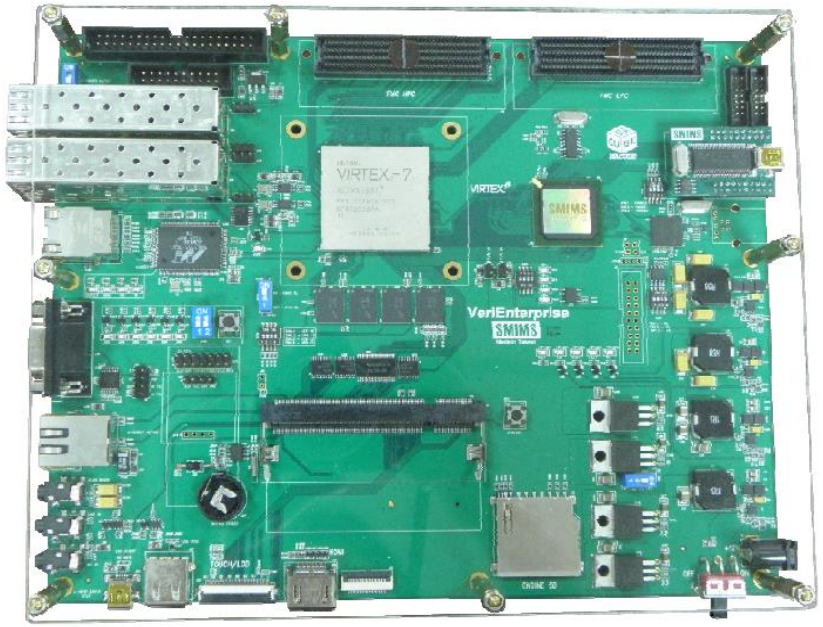
- This complete work will be in a package type of CQFP100.



Chip Layout Summary	
CMOS Technology	TSMC 40-nm
I/Q Wordlength	16 Bits
Core Utilization	0.8
Supply Voltage	0.99 V
SRAM Size	72704 Bits
Pin Count	96
Core Area	0.57 * 0.57 mm^2
Die Size	1.10 * 1.10 mm^2
Frequency	300.0 MHz
Power	45.34 mW

FPGA Prototyping

- The maximal clock operates at 89.6MHz in the Xilinx Virtex-7 XC7VX330T-ffg1157-3 FPGA platform.



Xilinx Virtex-7 FPGA Implementation Results

Resource	Used	Available	Utilization
Slice Registers	4,946	408,000	1.2%
Slice LUTs	14,213	204,000	7.0%
Memory	496	70,200	0.7%
Bonded IOBs	72	600	12.0%
RAMB36E1/FIFO36E1s	5	750	0.7%
RAMB18E1/FIFO18E1s	1	1,500	0.1%
BUFG/BUFGCTRLs	4	32	12.5%
DSP48E1s	64	1,120	5.7%

Design Comparison

	Proposed Work		[2]	[3]	[4]	[5]	[6]
FFT-Point Supporting	2 ~ 2187		12 ~ 1296	128/256/512/ 1024/1536/2048	128/256/512/ 1024/1536/2048	128/256/512/ 1024/1536/2048	1024
Max. FFT Size	2187		1296	2048	2048	2048	1024
Number of Mode	48		34	6	6	6	1
Process	40 nm		0.18 um	0.18 um	90 nm	65 nm	65 nm
Wordlength (Bit)	16		16	16	12	12	16
Core Area (mm^2)	0.300	0.325	25.000	1.932	0.783	1.375	8.299
Gate Count	354K	372K	482K	NA	205K	1,100K	NA
Frequency (MHz)	400.00	300.00	122.88	35.00	40.00	20.00	30.00
Throughput (M Symbols/s)	400.00	300.00	122.88	35.00	40.00	20.00	240.00
Power (mW)	39.00	45.34	320.00	11.29	7.20	8.55	4.14
Speed-Area Ratio (SAR) (10^{-3})	1.13	0.81	0.25	NA	0.20	0.02	NA
Power-Freq Ratio (PFR) (10^{-6})	44.58	69.11	2009.39	157.51	87.89	208.74	134.77
Implementation Results	Post-layout sim. (Macro layout)	Post-layout sim. (I/O PAD Limit)	Measurement	Measurement	Synthesis Results	Measurement	Measurement

▲ Speed-Area Ratio (SAR) $\triangleq \frac{\text{Throughput}}{\text{Gate\_Count}}$ ▲ Power-Freq Ratio (PFR) $\triangleq \frac{\text{Power}}{\text{Frequency} * \text{Max\_FFT\_Size}}$

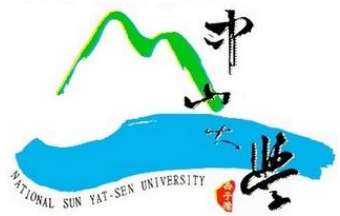
Critical Publications and Awards

- Journal publication:
  - X. Y. Shih, Y. Q. Liu, and H. R. Chou, "48-Mode Reconfigurable Design of SDF FFT Hardware Architecture Using Radix-3^2 and Radix-2^3 Design Approaches," ***IEEE Transactions on Circuits and Systems I: Regular Papers(TCAS-I)***, vol. 64, no. 6, pp. 1456-1467, June 2017.
  - X.-Y. Shih, H.-R. Chou, and Y.-Q. Liu, "VLSI Design and Implementation of Reconfigurable 46-Mode Combined-Radix Based FFT Hardware Architecture for 3GPP-LTE Applications," ***IEEE Transactions on Circuits and Systems I: Regular Papers(TCAS-I)*** , vol. 65, no. 1, pp. 118-129, Jan. 2018.
- Awards:
  - **2017 第十七屆旺宏金矽獎-設計組優勝獎**

Summary of Work I

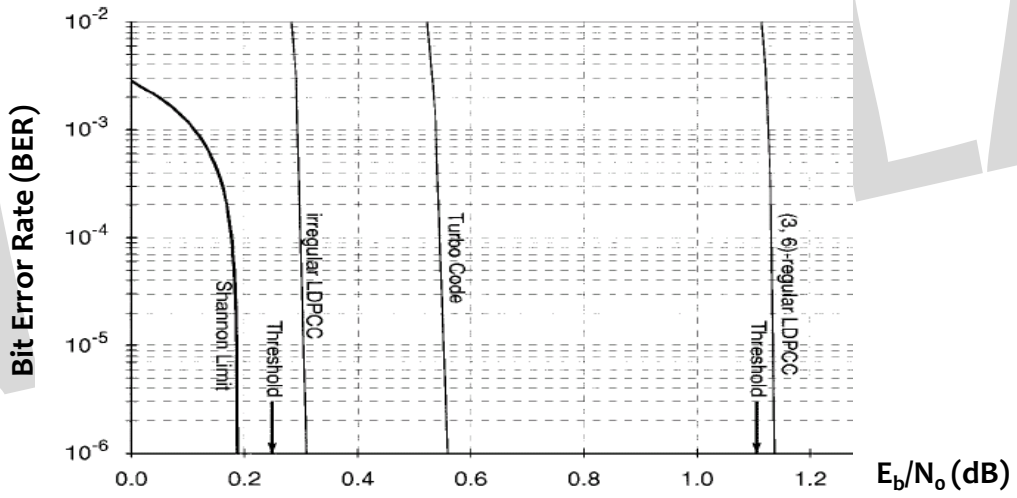
- What we propose :
  - **Reconfigurable LEGO-Based Hardware Architecture**
  - Design Techniques
    - T1 : 6-type Reconfigurable Processing Element (6T-RC-PE)
    - T2 : Systematic FIFO Reuse Arrangement (SFRA)
    - T3 : Section-based Twiddle Factor Generator (STFG)
- Chip features :
  - Modular/regular construction approach
  - Support 48 different FFT sizes (up to 2187 FFT points)
  - Hardware re-usage → Low area cost
  - High frequency
  - Green power

Work II : Efficient LDPC Decoder with On-Line Customized-Matrix Downloading



Low-Density Parity-Check (LDPC) Codes

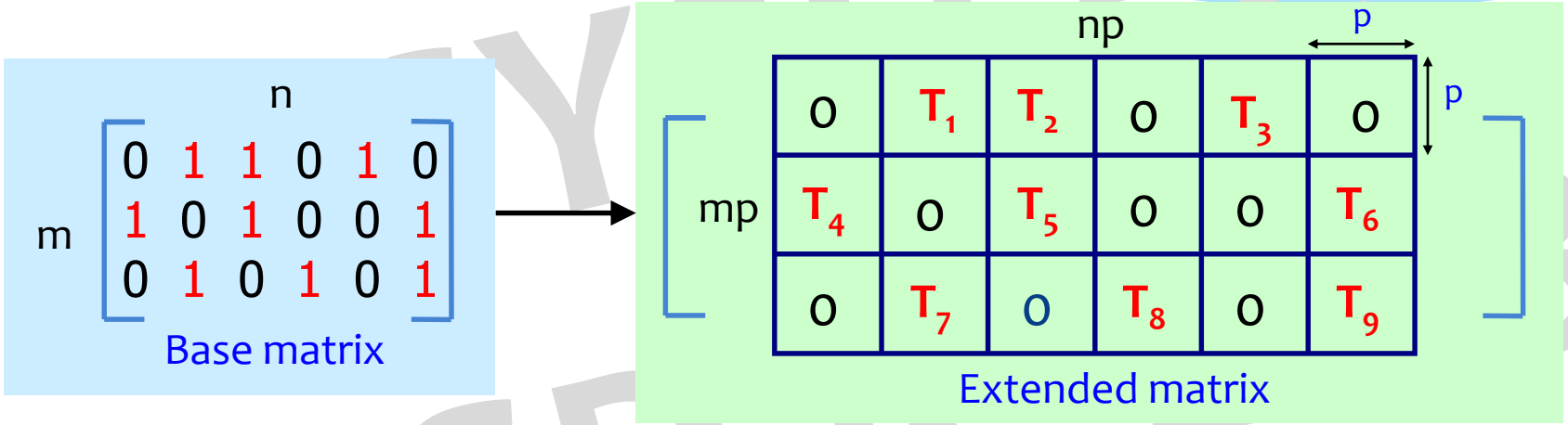
- First introduced by Gallager in 1962 [7]
- Rediscovered by MacKay in 1995 [8]:
  - Excellent error-correcting performance near the Shannon limit
  - Highly parallel decoding scheme
- With advanced VLSI technology, LDPC codes become more popular in advanced communication systems, IEEE 802.16e and 802.11n/ac/ax.



[8]

LDPC Encoding : Quasi-Cyclic (QC) LDPC

- Code construction of QC-LDPC codes:
  - $\mathbf{T}_i$ is the cyclic-shift matrix of the identity matrix I_p



[8]

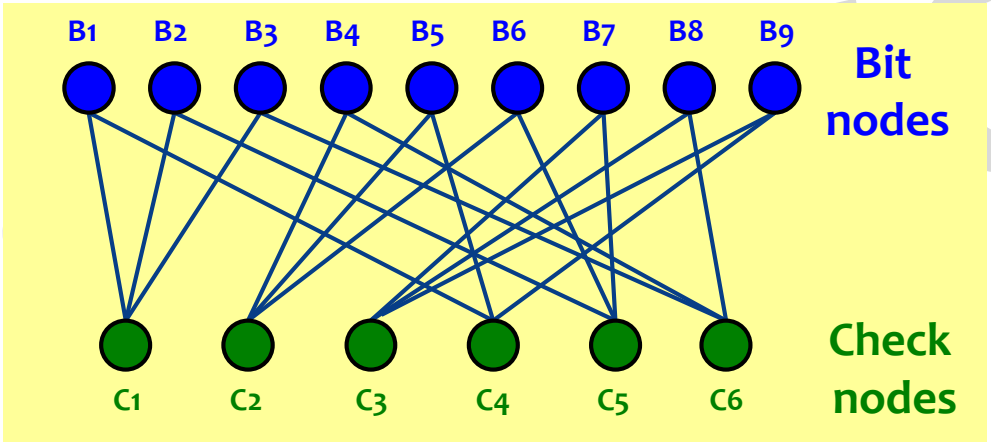
- Advantages:
  - Easier to handle the location of 1s.
  - Easily realized in partially-parallel method with storage elements.
  - Simple to manipulate the address access of the memory.

LDPC Decoding

- Parity check matrix

$$H = \begin{array}{c} \begin{matrix} B1 & B2 & B3 & B4 & B5 & B6 & B7 & B8 & B9 \end{matrix} \\ \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 0 \end{bmatrix} \end{array} \begin{matrix} C1 \\ C2 \\ C3 \\ C4 \\ C5 \\ C6 \end{matrix}$$

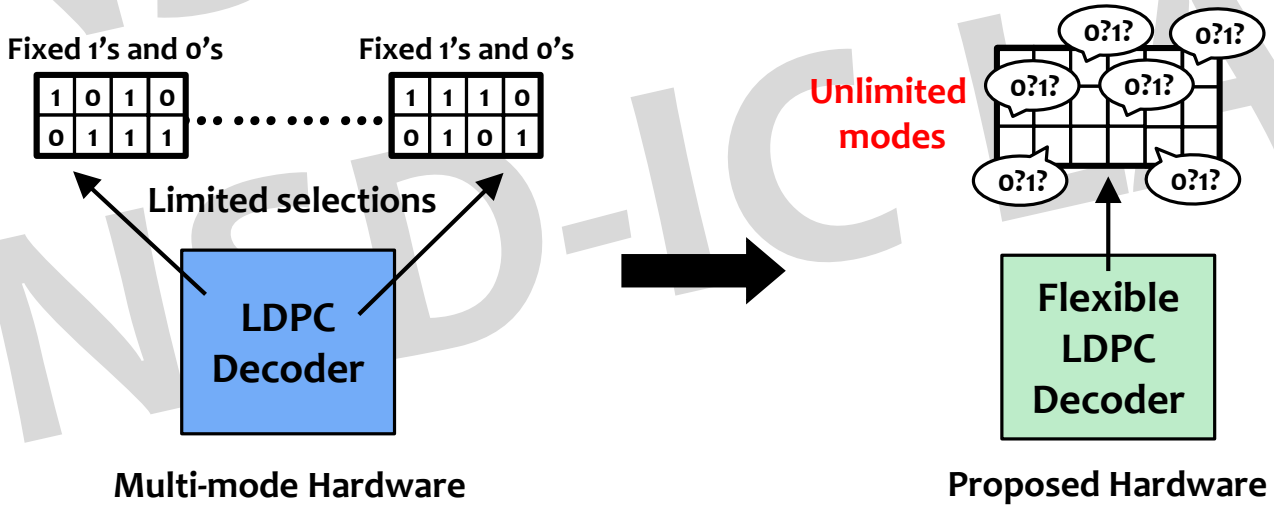
- Bipartite graph



- Decoding algorithms
  - Sum-Product Algorithm
  - Min-Sum Algorithm
  - Normalized Min-Sum Algorithm
  - **Layered Algorithm (V)**

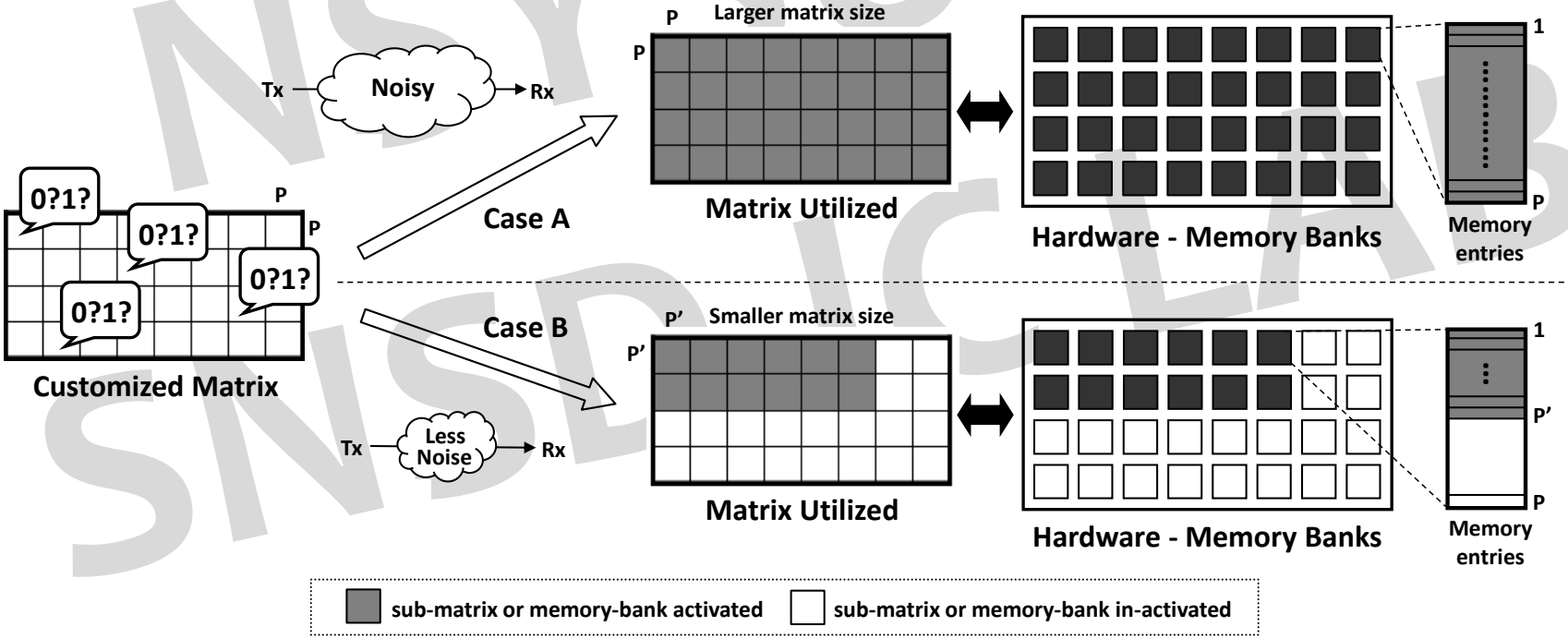
Proposed Flexible LDPC Hardware (1/3)

- Multi-mode design architecture : only support limited pre-defined matrices
- **Flexible design architecture** :
  - On-line download customized-matrix (ex. matrix size)
  - Adjust the location of 1's and 0's

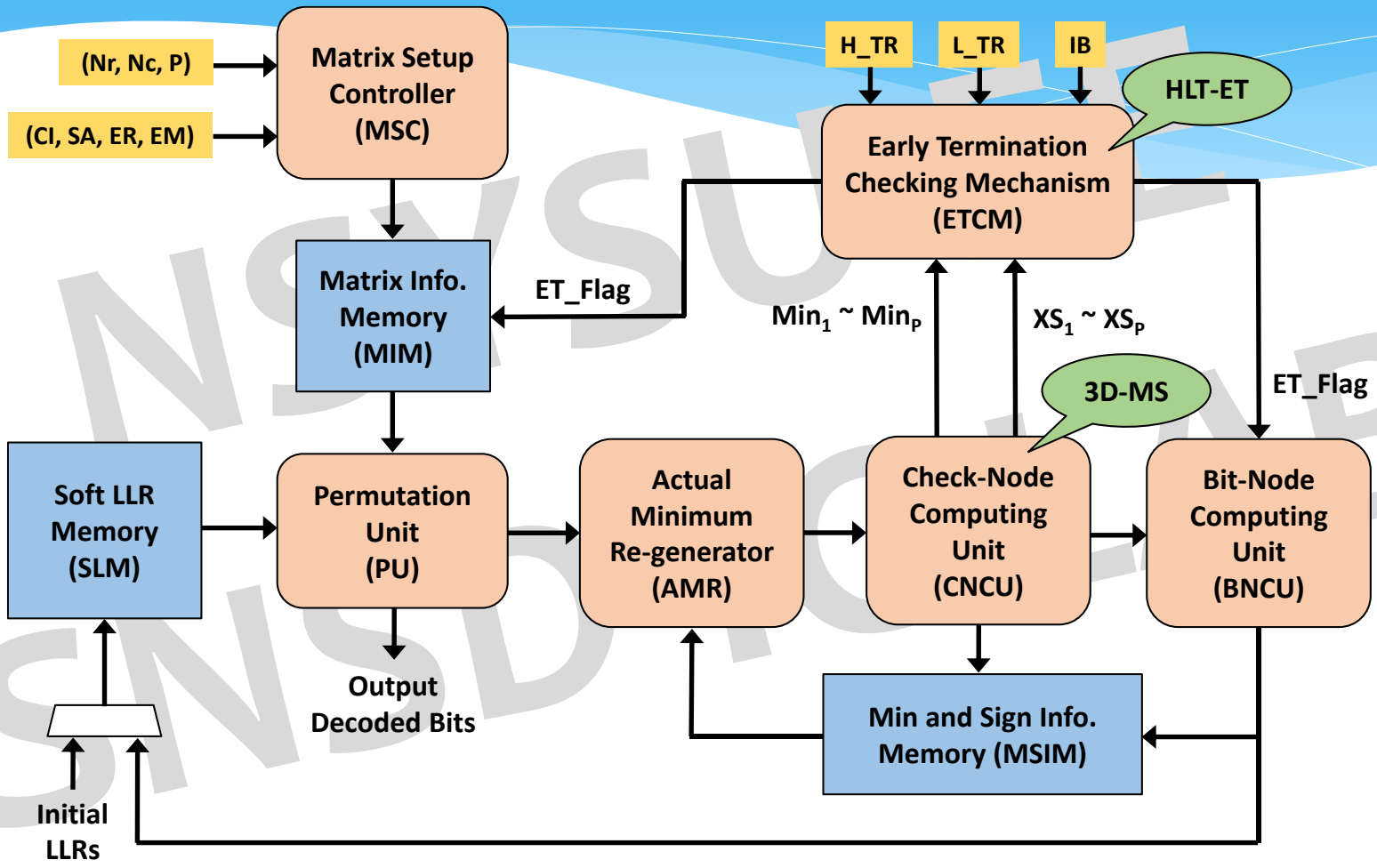


Proposed Flexible LDPC Hardware (2/3)

- Case A : In a long-distance transmission or noisy channel conditions, the architecture can be reconfigurable with larger codeword or lower code-rate.
- Case B : in a short-distance transmission or less-noise channel conditions, the architecture can be reconfigurable with shorter codeword or higher code-rate.



Proposed Flexible LDPC Hardware (3/3)



Example of A Customized Matrix

- (768, 384) LDPC codes : (Nr, Nc, P) = (4, 8, 96)
  - LDPC Matrix

	1	2	3	4	5	6	7	8
1	67	71		23	83	0		
2			46		9	0	0	
3	20	49			30		0	0
4		55	64	76	81	12		0

  - 20 clock cycles at **matrix-setup state** (before actual decoding)

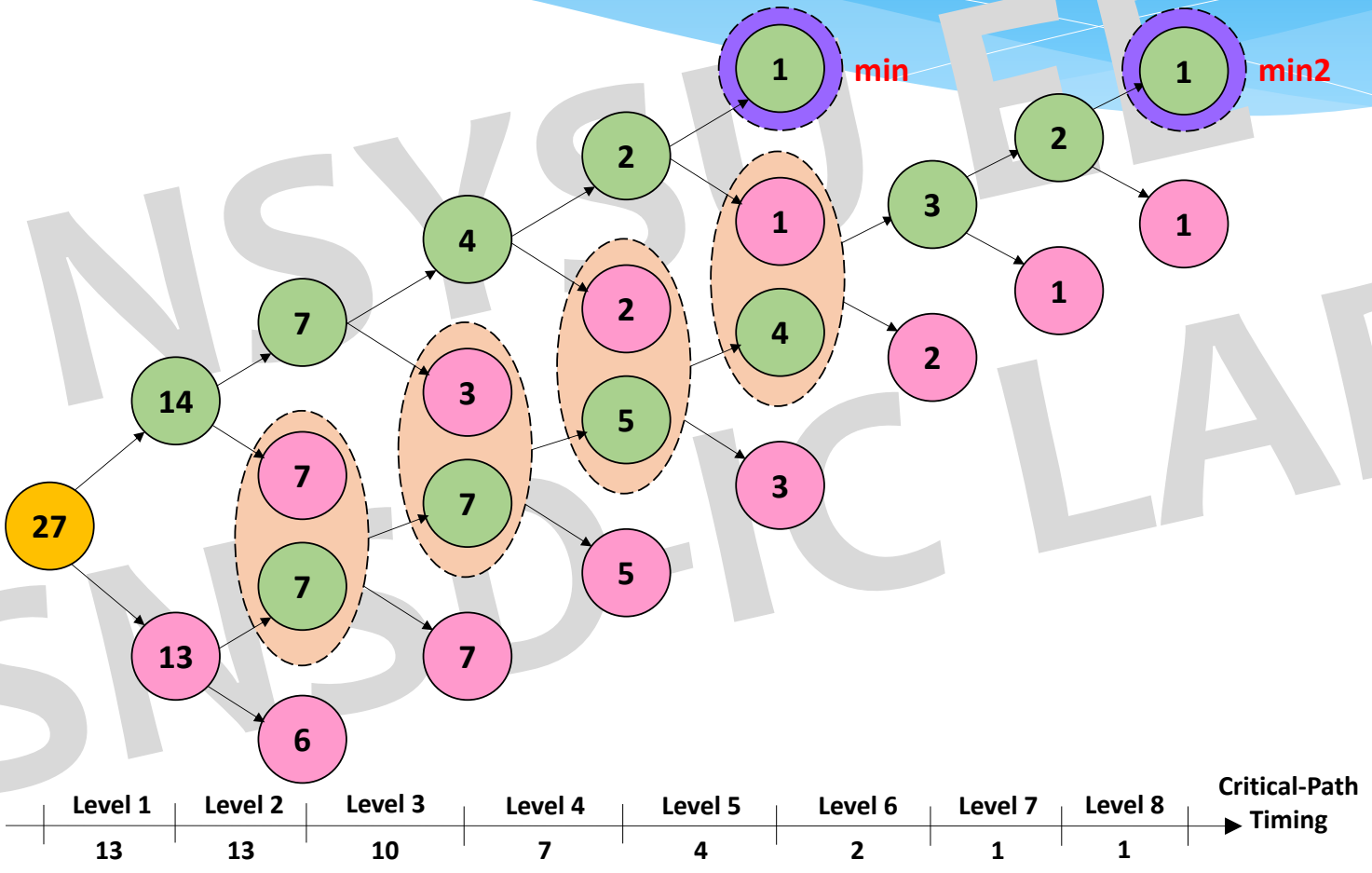
Time	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
CI	1	2	4	5	6	3	5	6	7	1	2	5	7	8	2	3	4	5	6	8
SA	67	71	23	83	0	46	9	0	0	20	49	30	0	0	55	64	76	81	12	0
ER	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	1
EM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Issue I : Longer Critical-Path Timing

- Motivation :
  - Check-node computing unit (CNCU) : need find **min** and **second min**
  - How to reduce the critical path while comparing large number of inputs? (ex. >= 20)
- Common comparison approach : Binary Search Trees (BST) [9]
  - Longer comparison process
  - Complex wire connection
- Proposed design approach : **3-Dimensional Minimum Searching (3D-MS)**
  - Shorter critical-path timing
  - Systematic and easily extensible

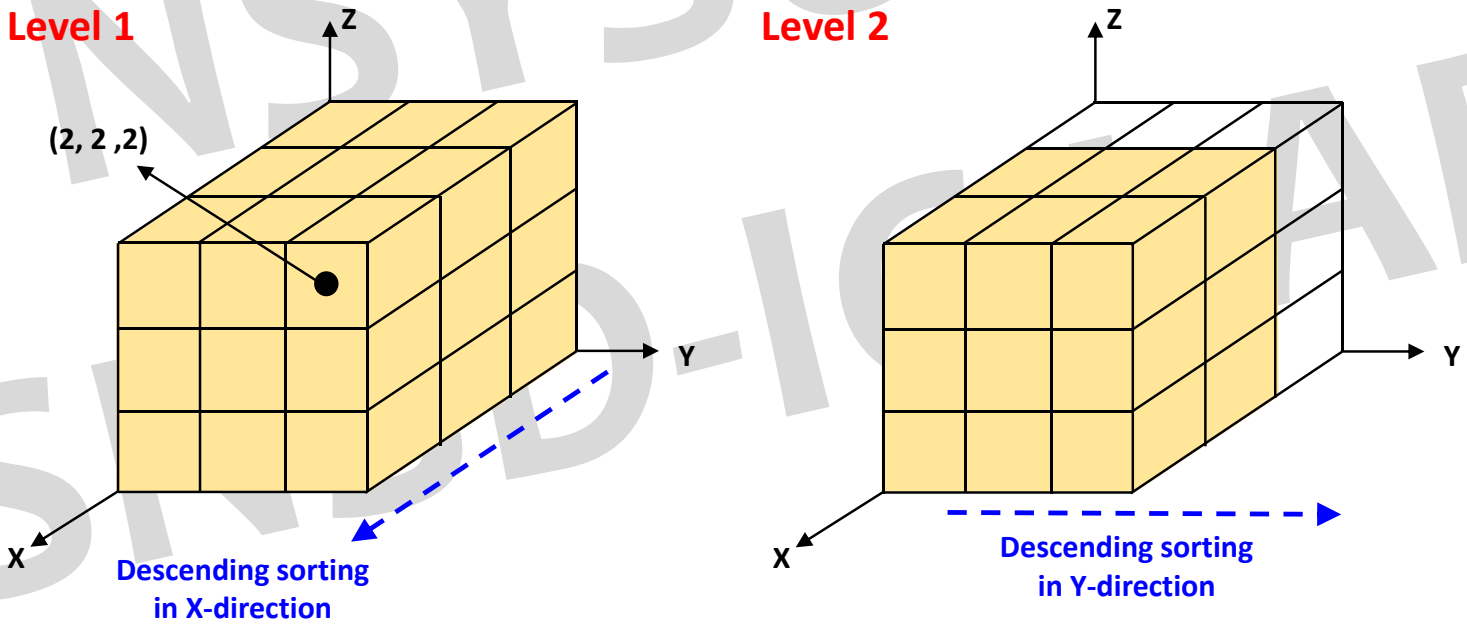
Binary Search Trees (BST) [9]

- EX. 27-input min/min2 finding : **8-level** subtractor comparison

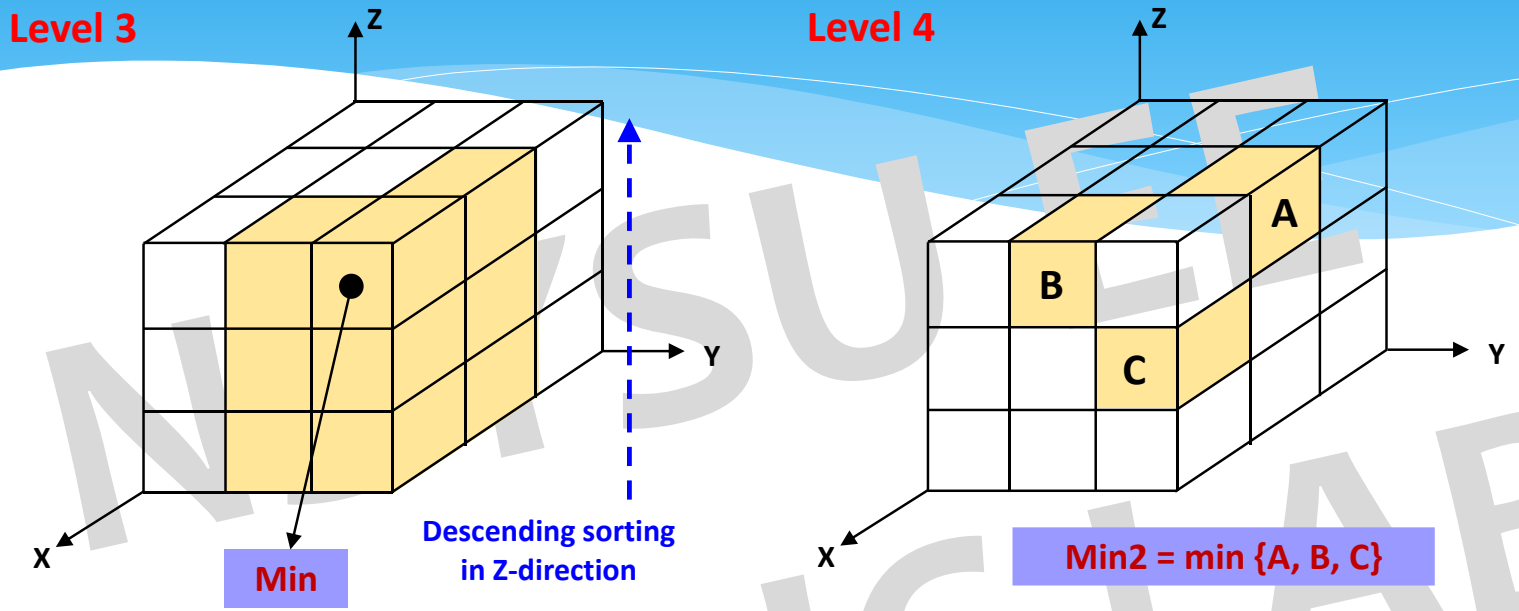


Proposed 3D-MS : 27-Input Design (1/2)

- 27 input candidates ： arbitrarily located in a 3-dimensional space, as a 3x3x3 cube.
- 4-level subtractor comparison process :



Proposed 3D-MS : 27-Input Design (2/2)



- Hardware resource :

Level	Sorting Points Activated		Sorting Direction	Number of Groups	Number of Subtractors Used		Note
	Number	List					
1	27	$\{(Px, Py, Pz) \mid 0 \le Px \le 2, 0 \le Py \le 2, 0 \le Pz \le 2\}$	X-axis	9	27	57	
2	18	$\{(1, Py, Pz), (2, Py, Pz) \mid 0 \le Py \le 2, 0 \le Pz \le 2\}$	Y-axis	6	18		
3	9	$\{(1, 2, Pz), (2, 1, Pz), (2, 2, Pz) \mid 0 \le Pz \le 2\}$	Z-axis	3	9		Find "Min"
4	3	$\{(1, 2, 2), (2, 1, 2), (2, 2, 1)\}$	-	1	3		Find "Min2"

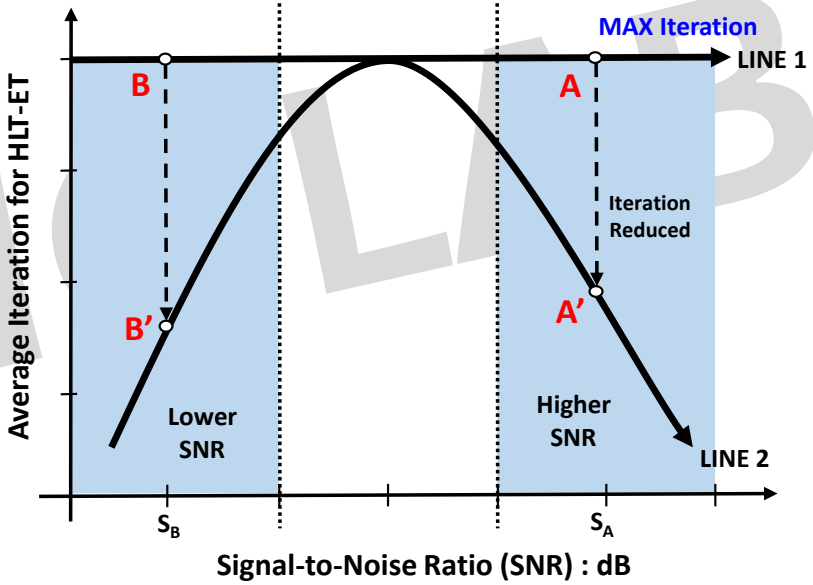
Comparison : 3D-MS v.s BST

- Pros of 3D-MS
  - Shorter critical-path time (33.3% ~ 50.0%)
  - Systematic and easily extensible
- Cons of 3D-MS
  - Hardware overhead (~10%)

Number of Inputs Compared		14	15	18	19	20	21	22	27	30
Different Standard Supported	IEEE 802.16e	V	V			V				
	IEEE 802.11n/ac/ax	V	V		V	V	V	V		
	DVB-S2	V		V	V			V	V	V
Critical-Path Timing	BST	6	6	7	7	7	7	7	8	8
	3D-MS	4	4	4	4	4	4	4	4	5
Subtractors Utilized	BST	25	27	33	35	37	39	41	51	57
	3D-MS	27	29	36	39	41	43	46	57	62
Critical-Path Timing Reduced Ratio		33.3%	33.3%	42.9%	42.9%	42.9%	42.9%	42.9%	50.0%	37.5%
Hardware Overhead (Subtractors)		8.0%	7.4%	9.1%	11.4%	10.8%	10.3%	12.2%	11.8%	8.8%

Issue II : Inefficient LDPC Decoding

- Decoding phenomenon :
  - For any SNR regions, it is decoded with the same iteration number --> inefficient decoding & power waste
- Motivation of reducing iteration number :
  - Higher-SNR region :
    - Without performance loss
  - Lower-SNR region :
    - Facing noisy channel conditions
- Proposed approach :
  - **High-and-Low-Thresholds Based Early Termination (HLT-ET)**



Proposed HLT-ET : Design Flow

- Adjustable parameters :

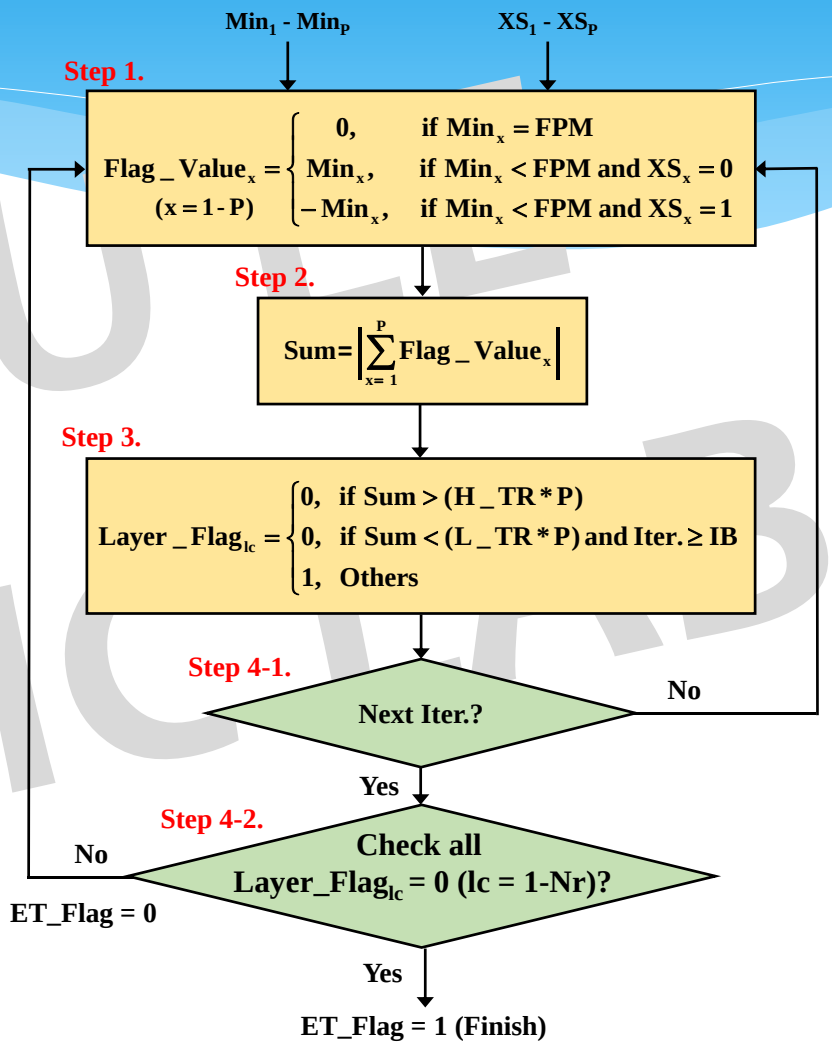
  H_TR : High threshold
  L_TR : Low threshold
  IB = Iteration boundary for ET-checking

- Symbol/notation :

  FPM : max of fixed-point representation
  P = Sub-matrix size
  lc = Layer count

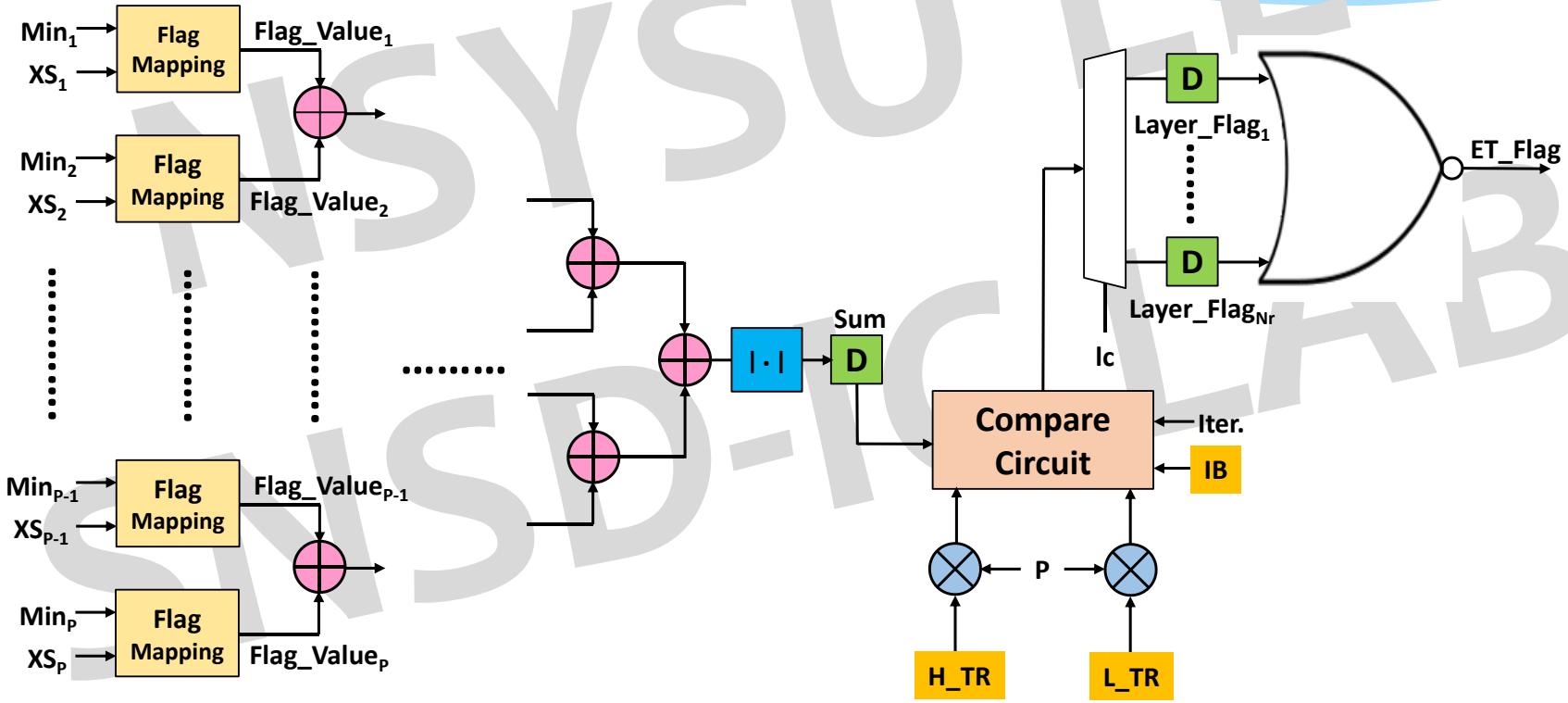
- Suggested values :

  Decide from Experiment :
  H_TR = 5
  L_TR = 2
  IB = 3



Proposed HLT-ET : Hardware Circuits

- Detailed hardware circuits of HLT-ET



Parameters for Proposed Hardware

Adjustable parameters :

Design configuration parameters:

Signal	Meaning for Parameter Controlling	Range
Nr	Row count of base parity check matrix	[1, 12]
Nc	Column count of base parity check matrix	[1, 27]
P	Sub-matrix size or extending factor	[1, 96]
CI	Column index of non-blank element	[1, 27]
SA	Shifted-right amount of non-blank element	[0, 95]
ER	Indicator of the end of row	0 or 1
EM	Indicator of the end of matrix	0 or 1
MIC	Max of iteration count	[1, 8]

Early termination checking parameters:

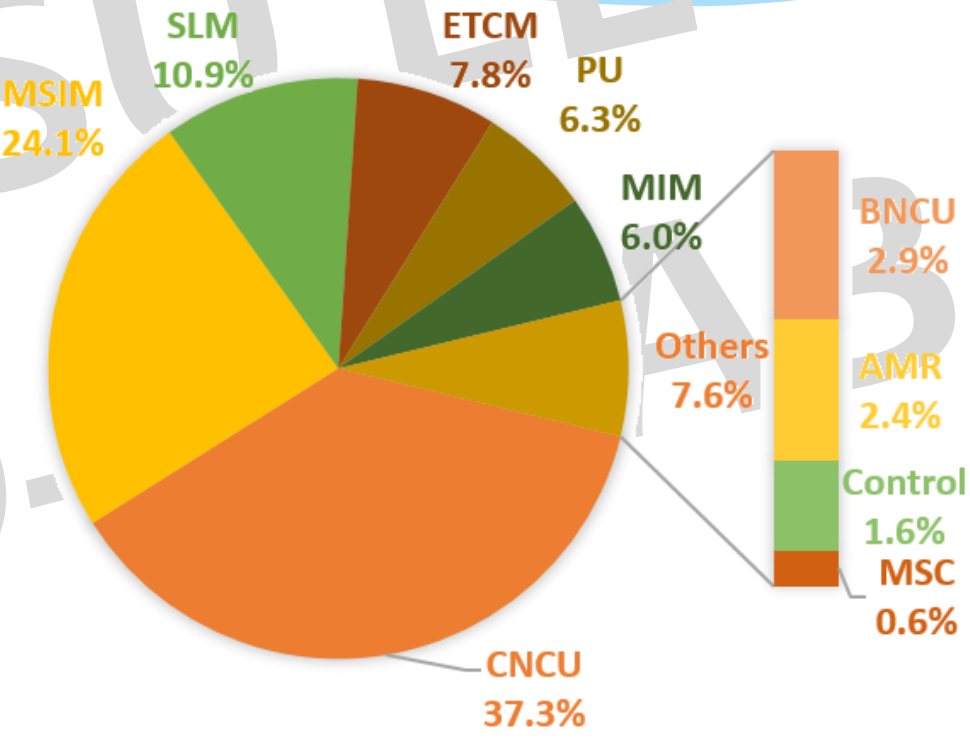
Signal	Meaning for Parameter Controlling	Range
H_TR	High threshold for checking high-SNR zone	[0, 7]
L_TR	Low threshold for checking low-SNR zone	[0, 7]
IB	Iteration boundary for ET-checking	[0, 8]

Synthesis Results

- Design summary:

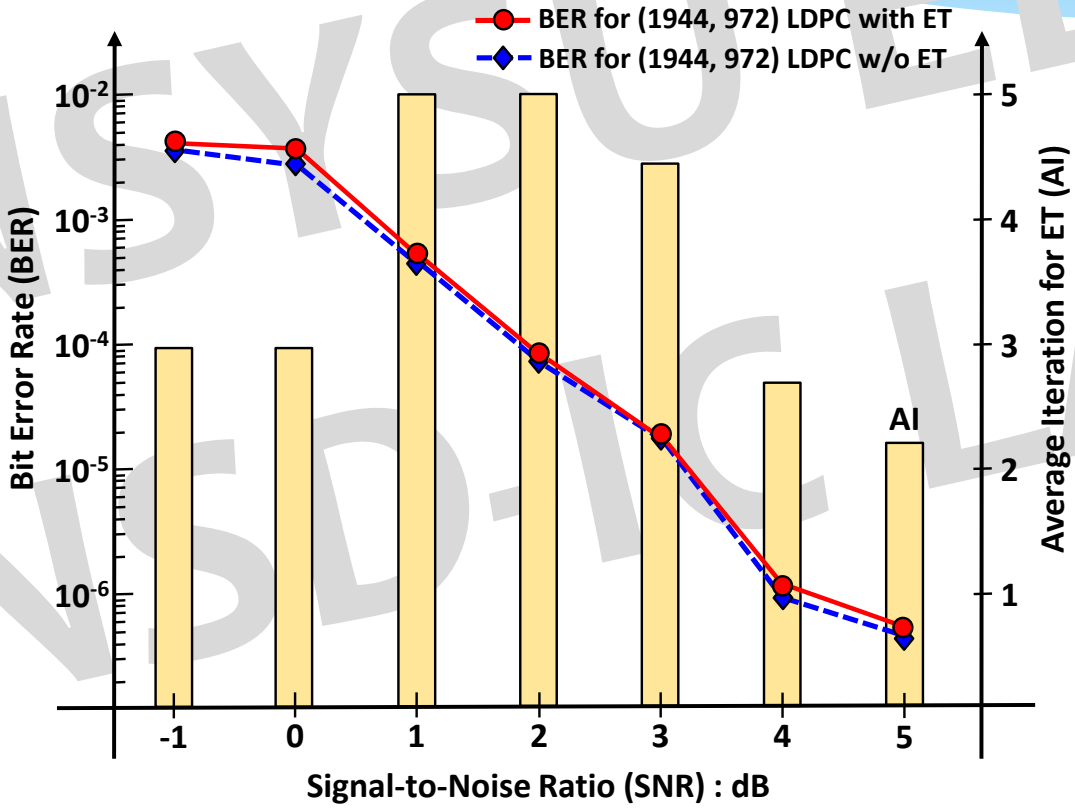
Number of Modes	Un-limited (Flexible)
Parameters Supported	non-limited
Decoding Algorithm	Layered Decoding
Technology	TSMC 40-nm CMOS Process
Max Codeword Length	2592 bits
Wordlength	6 bits
Supply Voltage	0.9 V
SRAM Size	58.368 Kbits
Operating Frequency	1.0 GHz
Occupied Area	0.415 mm^2
Max Throughput	1.4 Gbps (with HLT-ET)
Power Dissipation	84.68 mW

- Area details:



System Verification

- IEEE 802.11ax : (1944, 972) LDPC codes
  - Parameter Setting : (MIC, H_TR, L_TR, IB) = (5, 5, 2, 3)



Design Comparison

	DATE [10]	JSSC [11]	TCAS-I [12]	TCAS-II [13]	SOCC [14]	TCAS-I [15]	Proposed
Decoding Algorithm	Layered	MSA	Modified TDMP	MSA	BP	Modified MSA	Layered
Standard Supported	16e	16e	16e/11n	16e/11n	16e/11n	16e/11n/G.hn	(Customized)
Number of Modes	114	114	114 + 12	114 + 12	114 + 12	114 + 12 + 7	(Un-limited)
Process Technology	65nm	90nm	180nm	90nm	90nm	90nm	40nm
Supply Voltage (V)	1.2	1.0	1.8	1.0	1.0	1.0	0.9
Max Codeword (Bits)	2304	2304	2304	2304	2304	8640	2592
Quantization (Bits)	6	6	6	9	*NA*	6	6
Number of Iteration	10 - 15	20	10	20	10	8 - 12	1 - 5
Frequency (MHz)	400	150	100	300	450	400	1000
Design Area (mm^2)	1.337	6.250	10.120	6.220	3.500	5.529	0.415
Total Gate Count	*NA*	970K	463K	947K	*NA*	*NA*	610K
Power (mW)	*NA*	264.00	856.00	528.00	410.00	517.70	84.68
Max Throughput (Mbps)	333	105	168	212	1000	1957	1400
NAE (bit/mm^2) [16]	0.156	0.054	0.318	0.054	0.304	0.424	0.319
NEE (nJ/bit) [16]	*NA*	7.554	1.181	7.483	1.232	0.795	1.136

▲ NAE = Normalized Area Efficiency ▲ NEE = Normalized Energy Efficiency

Critical Publications and Awards

- Conference publication:
  - Xin-Yu Shih and Yu-Chun Chen, "2-Dimensional Minimum Fast-Searching Design Approach of LDPC Decoder Architecture for IEEE 802.11n/ac/ax Applications," in *IEEE International Conference on Consumer Electronics - Taiwan (2017 IEEE ICCE-TW)*, 2017, pp. 119-120.
  - Xin-Yu Shih, "XYZ-Direction Fast Minimum Searching Approach of High-Row-Weight LDPC Decoders for Advanced Communication Applications," in *The 5th Seoul International Conference on Applied Science and Engineering (2017 SICASE)*, December 2017, pp. 226-227.
- Awards:
  - **2017 光電與通訊工程應用研討會最佳論文獎**

Summary of Work II

- What we propose :
  - **Flexible design architecture**
    - On-line download customized-matrix (ex. matrix size)
    - Adjust the location of 1's and 0's
  - Design Techniques
    - T1 : 3-Dimensional Minimum Searching (3D-MS)
    - T2 : High-and-Low-Thresholds Based Early Termination (HLT-ET)
- Chip features :
  - On-line download customized-matrix
  - Reduced critical-path timing
  - Efficient LDPC decoding

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Many thanks for your listening!

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