Phase-Locked Loop Design and Applications

(鎖相迴路的設計與應用)

國立高雄師範大學 電子工程學系

羅有龍

Outline

- Introduction
- PLL Applications
- Design Considerations of PLL
- Proposed Low-Voltage PLL
- Conclusions

Outline

- **Introduction**
  - **Semiconductor Brief History**
  - **Full Custom IC Design Concept**
- **PLL Applications**
- **Design Considerations of PLL**
- **Proposed Low-Voltage PLL**
- **Conclusions**

Q&A

- What is Semiconductor?
- What is IC?

Semiconductor Brief History

- **Mechanical Era (1623-1945)**

1906 **Vacuum Tube (Lee Deforest).**

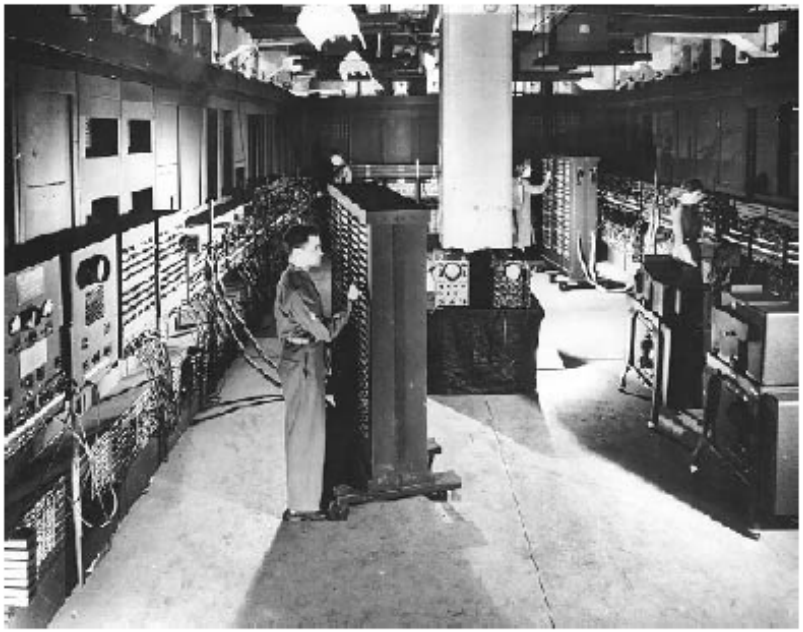
Three elements device used as electronic switch and amplifier: two electrodes separated by a grid in a vacuum glass enclosure.

Semiconductor Brief History (cont'd)

- **Mechanical Era (1623-1945)**

1943 **British built code-breaking Vacuum Tube Computer called Colossus.**

WWII **Americans built a general purpose electronic computer, prior to that John Atanasoff built an Electromechanical Digital Computer with some vacuum tube.**



•18,000 electron tubes
•19000 additions/s

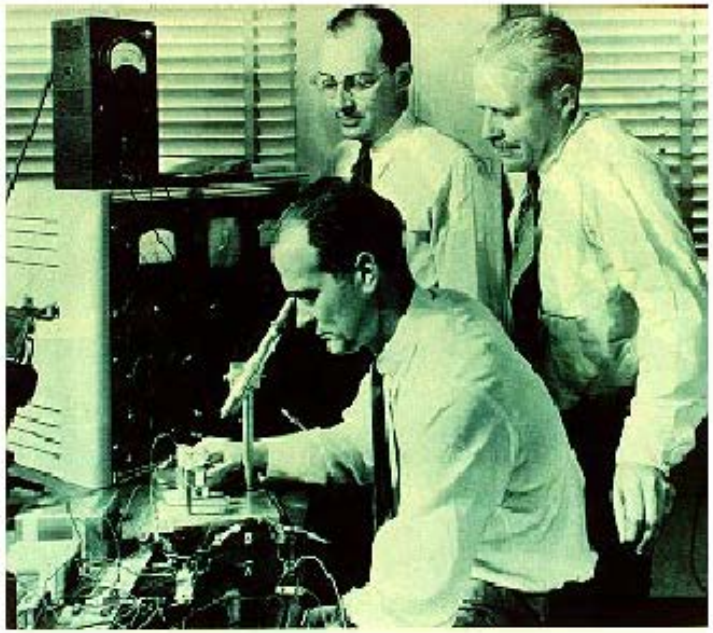
Electronic Numerical Integrator and Computer

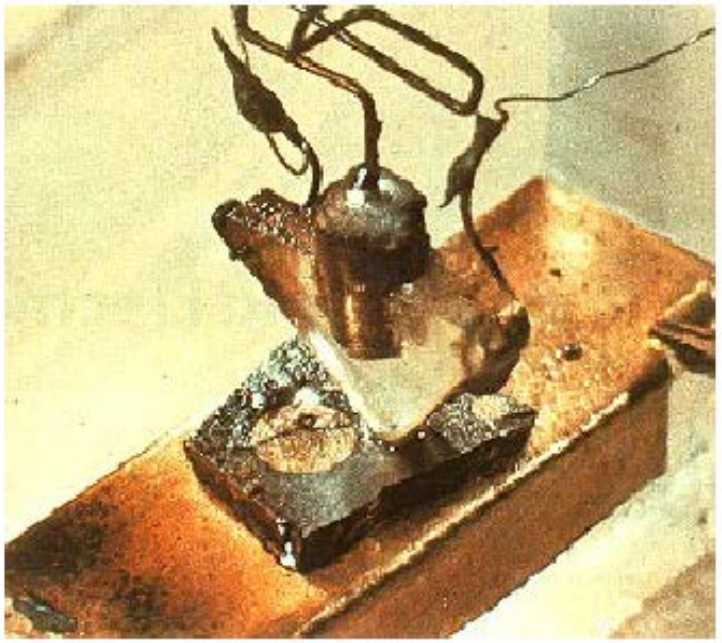
To calculate ballistic missiles trajectories

Semiconductor Brief History (cont'd)

- **Semiconductor Era (1947-21th century)**

1947 **First transistor designed by John Bardeen, Walter Brattain and William Shockley for Bell Labs . (Nobel prize in 1956)**

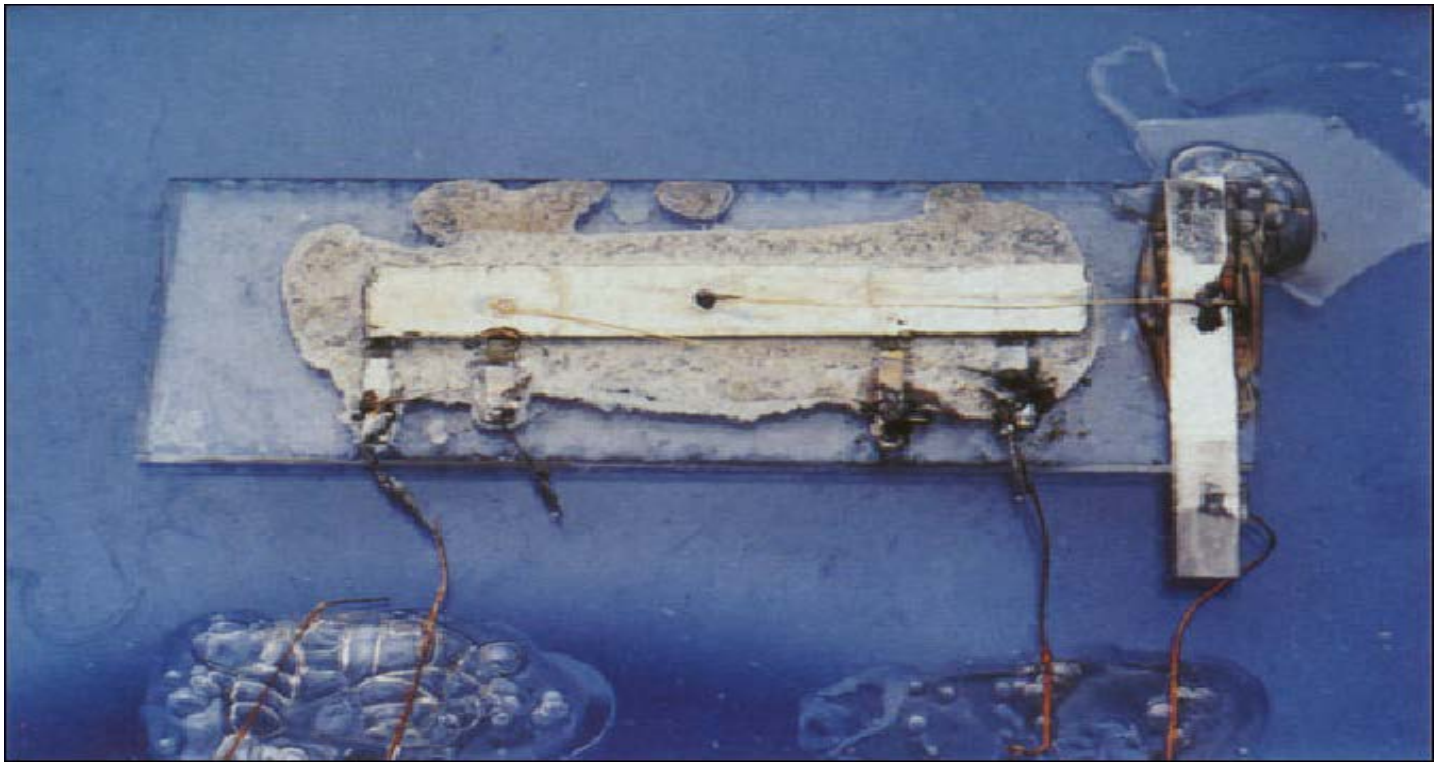




Semiconductor Brief History (cont'd)

- **Semiconductor Era (1947-21th century)**

1958 Jack Kilby at Texas Instrument had built **first semiconductor IC** separately. The simple oscillator IC with five integrated components (resistors, capacitors, distributed capacitors and transistors).

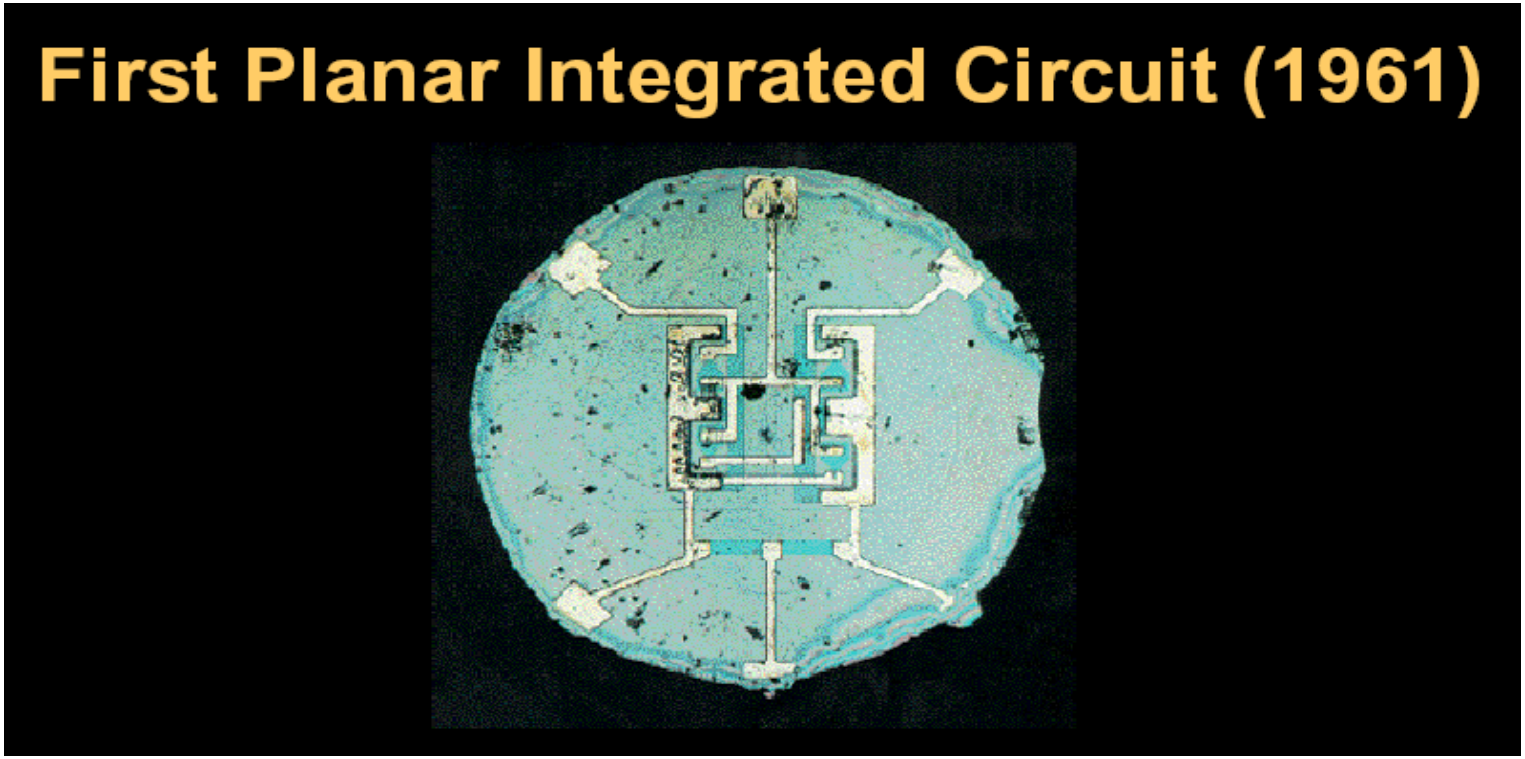


A simple oscillator IC

Semiconductor Brief History (cont'd)

- **Semiconductor Era (1947-21th century)**

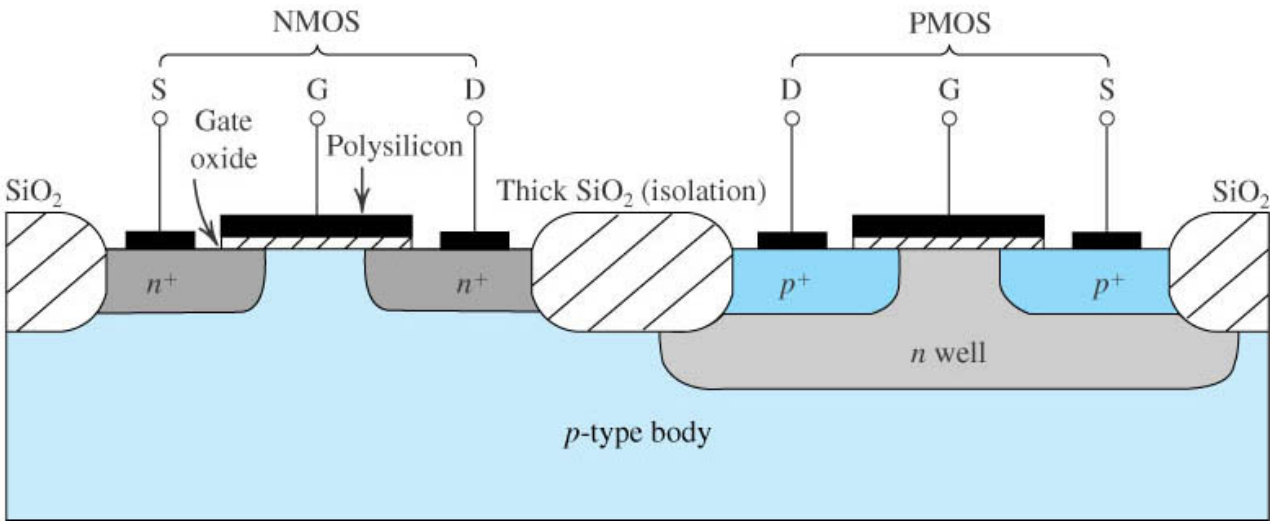
1961 Jean Hoerni at Fairchild semiconductor had developed first planar IC. Entire wafer is a single transistor.

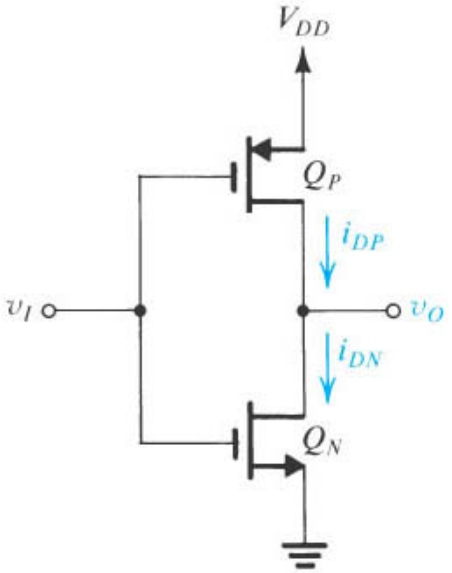


Semiconductor Brief History (cont'd)

- **Semiconductor Era (1947-21th century)**

1963 **CMOS invented by Frank Wanlass at Fairchild semiconductor originated and published the idea of Complementary-MOS (CMOS). CMOS forms the basis of the vast majority of all high density ICs manufactured today.**



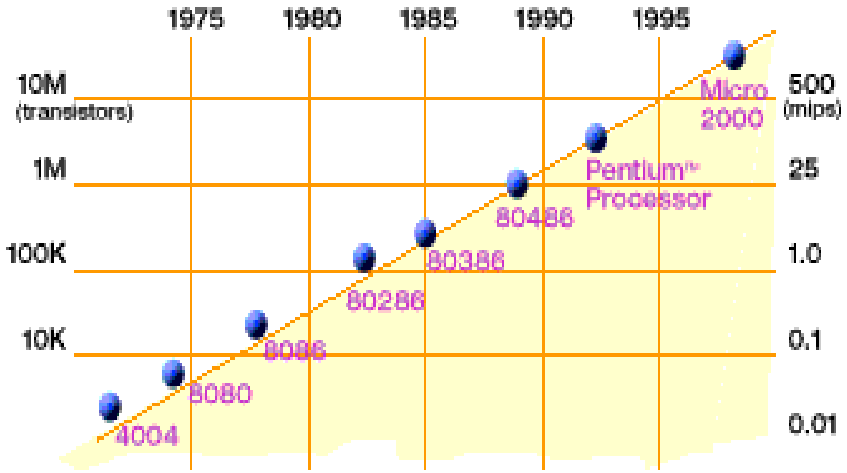


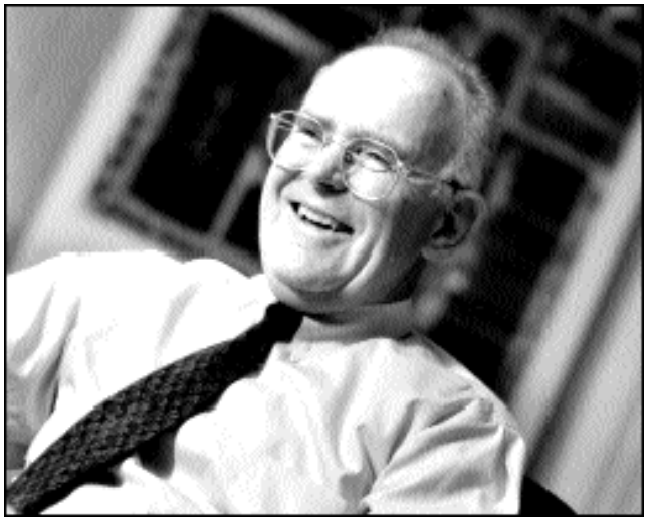
Metal-Oxide-Semiconductor (MOS) Field-Effect-Transistor (FET)

Semiconductor Brief History (cont'd)

- **Semiconductor Era (1947-21th century)**

1965 **Moore's Law**





2X transistors/Chip Every 1.5 years
Called "Moore's Law"
Microprocessors have become smaller, denser, and more powerful.

Gordon Moore (co-founder of Intel) predicted in 1965 that the transistor density of semiconductor chips would double roughly every 18 months.

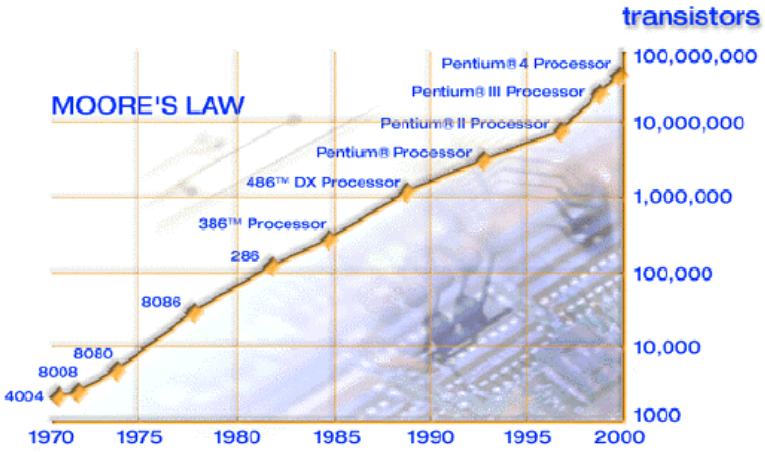
Semiconductor Brief History (cont'd)

- **Semiconductor Era (1947-21th century)**

1968 **Noyce and Moore founded Intel**

- Moore's law is good for many years!

1971: 4004	2,250 transistors
1972: 8008	2,500 transistors
1974: 8080	5,000 transistors
1978: 8086	29,000 transistors
1982: 80286	120,000 transistors
1985: 80386	275,000 transistors
1989: 80486 DX	1,180,000 transistors
1993: Pentium	3,100,000 transistors
1997: Pentium II	7,500,000 transistors
1999: Pentium III	24,000,000 transistors
2000: Pentium IV	42,000,000 transistors
2002: Itanium	325,000,000 transistors (25M CPU / 300M Cache)



Semiconductor Brief History (cont'd)

- **Semiconductor in Our Life**

Harzoom
MP3 Player

In-Car Digital Player

Ericsson
Screenphone

Nintendo
Gameboy Advance

IBM

Linux watch

Litronic Forté Card

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- **Introduction**
  - Semiconductor Brief History
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- PLL Applications
- Design Considerations of PLL
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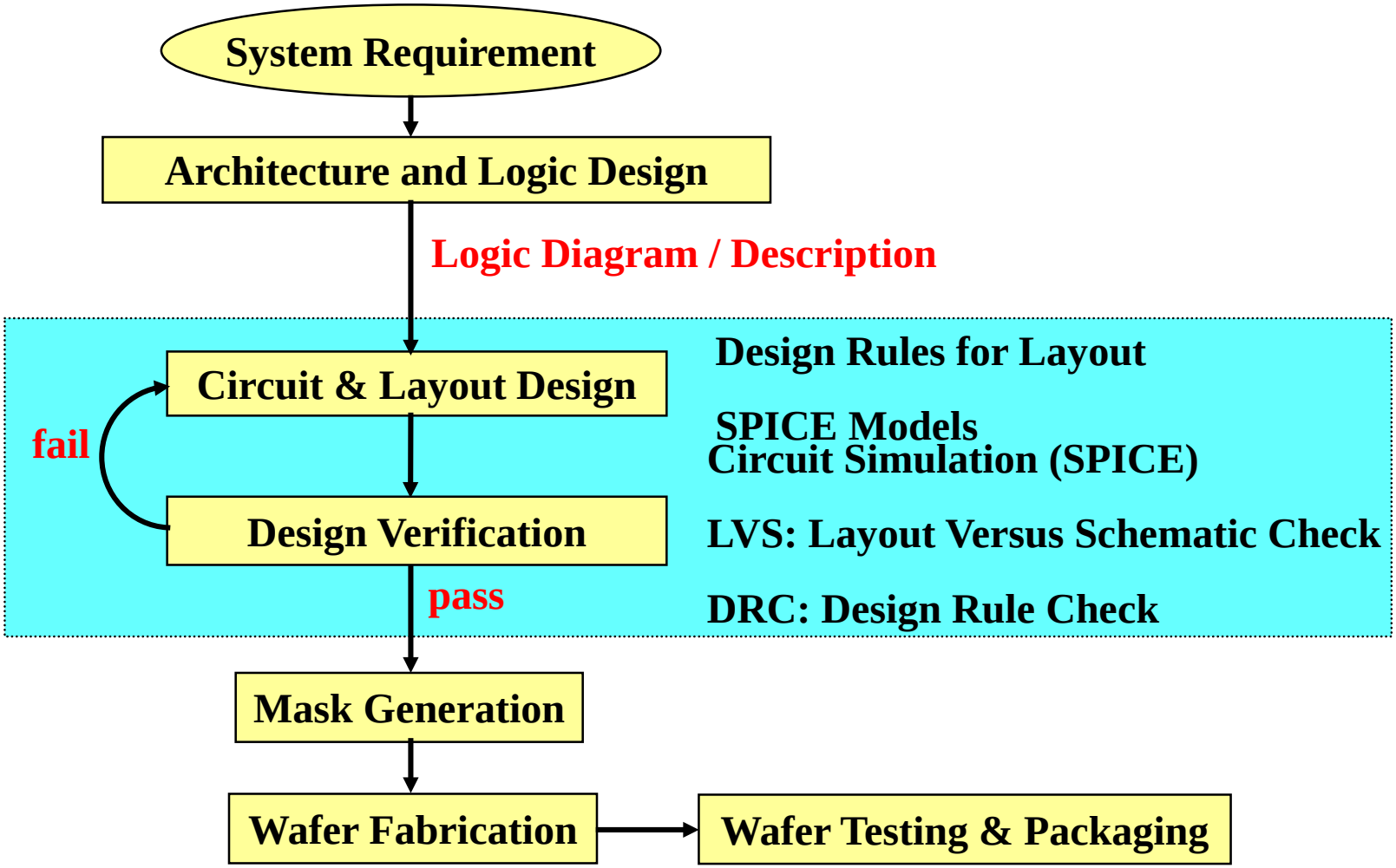
Full Custom IC Design Concept

- **Design Styles**
  - **Full Custom Design Flow**
    - ✓ Circuit is created by composing a transistor netlist
    - ✓ SPICE simulation is performed to verify the circuit
    - ✓ Layout is mostly done manually
    - ✓ Popular for high-performance microprocessors & memories
  - **Cell-Based Synthesis Flow**
    - ✓ Design is first described by Hardware Description Language (e.g., Verilog and VHDL)
    - ✓ Based on a cell library, netlist is created by synthesis tools
    - ✓ Layout can be done through automatic tools

Full Custom IC Design Concept (cont'd)

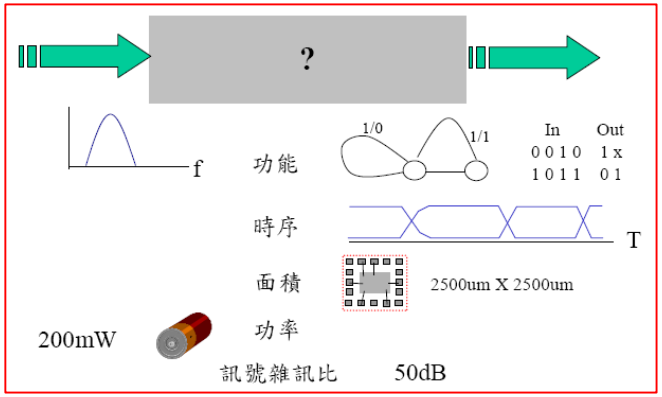
- **Custom Design Flow**



Full Custom IC Design Concept (cont'd)

IC Design Step

- 規格定義 需求時脈頻率，輸出入時序、功能對應...
- 製程選擇 (0.35/0.25/0.18, logic, mixed-mode, Embed)CMOS, BiCMOS,GaAs
- 架構選擇 Dynamic/Static logic, Parallel/Serial/Pipelined ...
- 電路設計 模組分割，需求定義，電路方塊設計與連接
- 電路模擬 功能模擬，時序驗證...
- 佈局設計 Auto Placement&Route(APR), HandCraft, Using Hard IP
- 佈局驗證 DRC/ERC, LVS, ...
- 佈局後模擬 LPE， Delay Calculation , Backannotation
- 可靠性分析 Electron-migration, ESD, Substrate coupling ...



Ref: CIC's course "Full Custom IC Design Concepts"

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  - **What is PLL?**
  - How Are PLL's Used?
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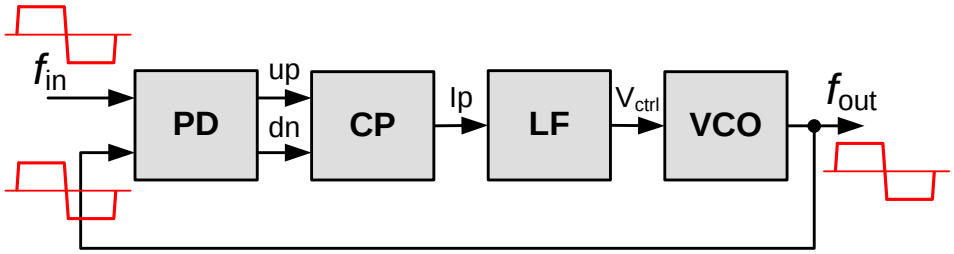
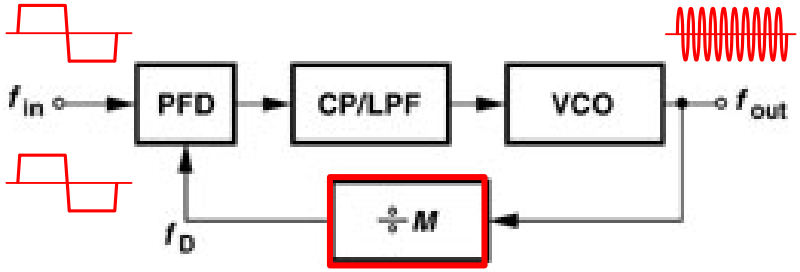
What is PLL?

- **PLL Blocks**





-Phase Detector (PD) / Phase Frequency Detector (PFD)

-Charge Pump (CP)

-Loop Filter (LF) / Low Pass Filter (LPF)

-Voltage-Controlled Oscillator (VCO)

-Divider (/M)

$f_{out}=Mf_{in}$

- A PLL is a "negative feedback system" where an oscillator-generated signal is phase and frequency locked to a reference signal
- Analogous to a car's "cruise control"

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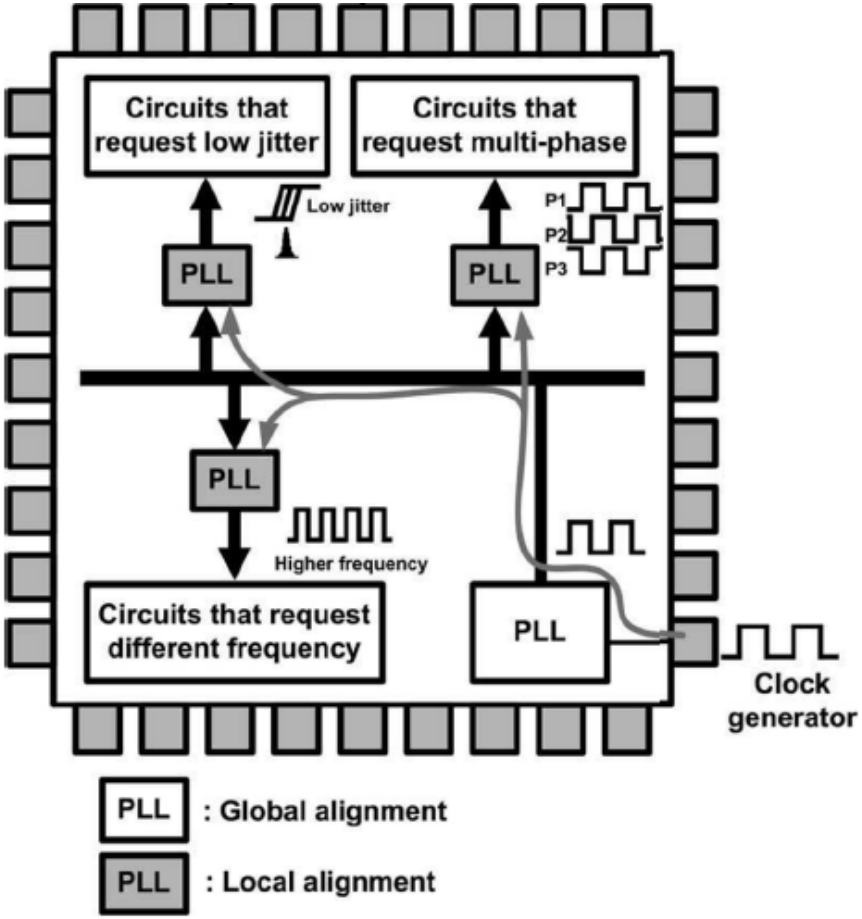
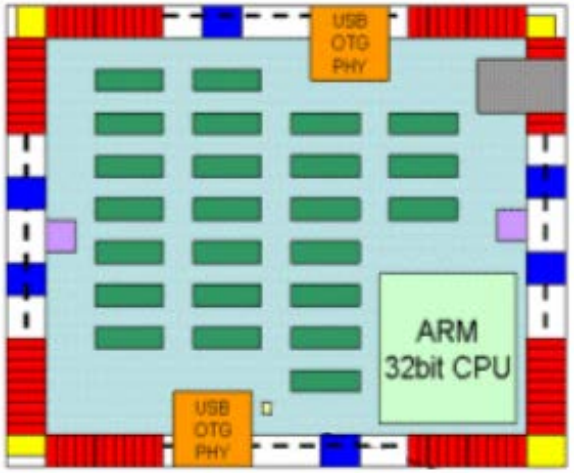
How Are PLL's Used?

- **PLL Application in SoC**



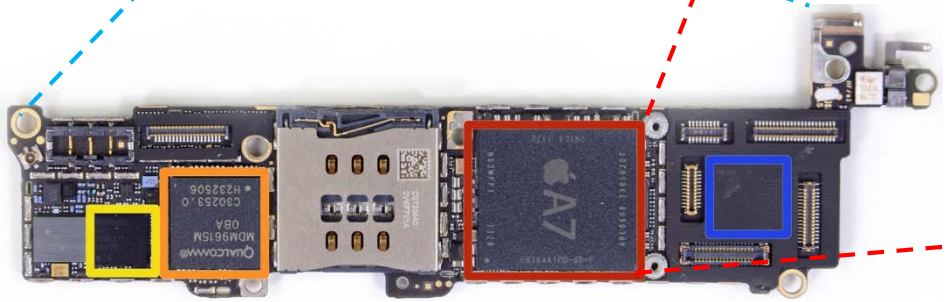


Configurations	FIT9400	FIT9500	FIT9600	FIT9700	FIT9800
MPCA size	1024K	2236K	2048K	4352K	6400K
RAM bits	768K	1536K	1644K	2560K	4224K
#PLL	4	4	6	8	12
#DLL	2	2	2	4	4
32 bit CPU	0	0	1	0	0
USB PHY	1	1	2	2	2
E h 10/100	0	0	1	0	1
Analog IP	*	*	*	*	*
# MPIO	292	388	484	484	580

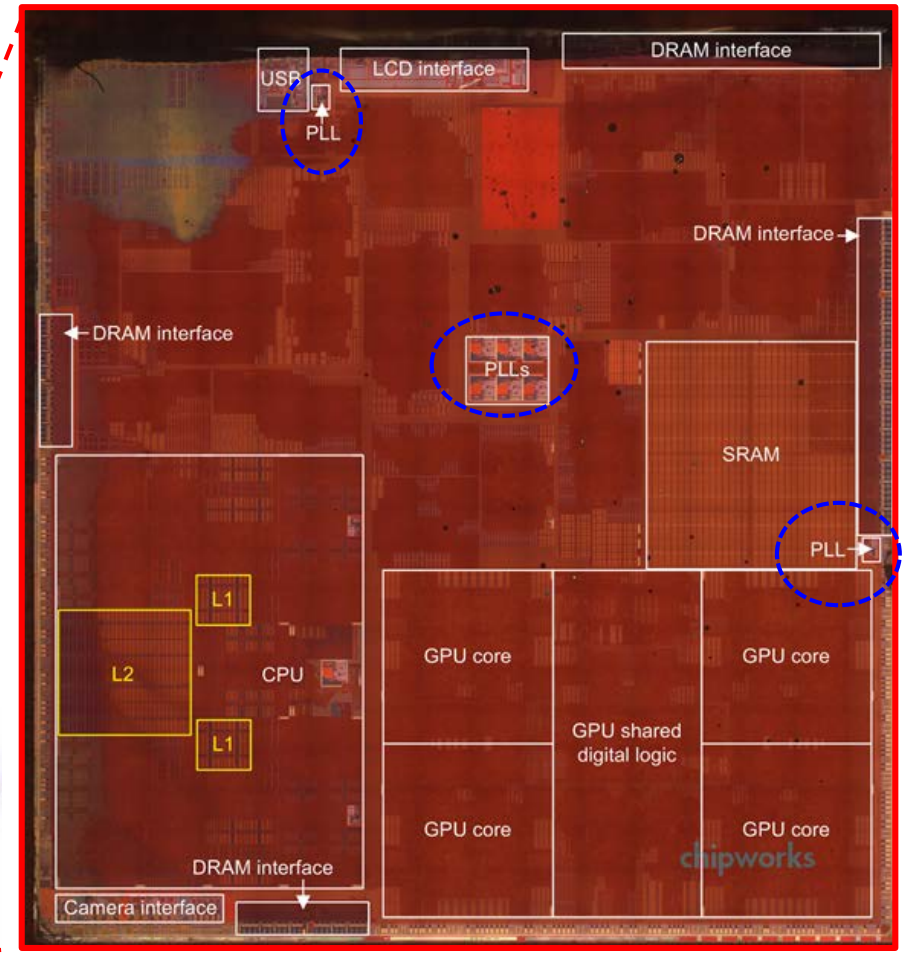
source:http://vda.ee.nctu.edu.tw/EDAF/monthly_letter/sasic.pdf

How Are PLL's Used? (cont'd)

- **iPhone 5s**



Operating frequency: 1.3GHz



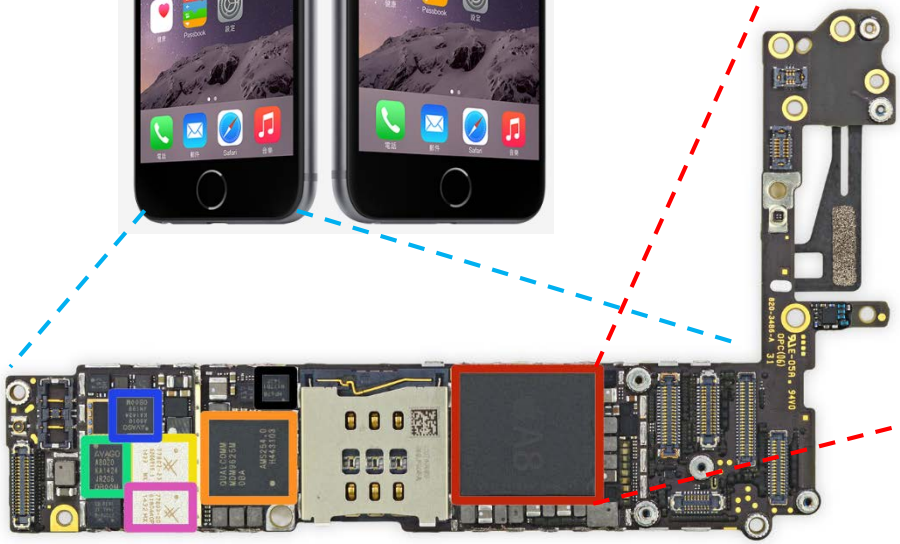
Apple A7 Processor Floorplan

https://www.ifixit.com/Device/iPhone_5s

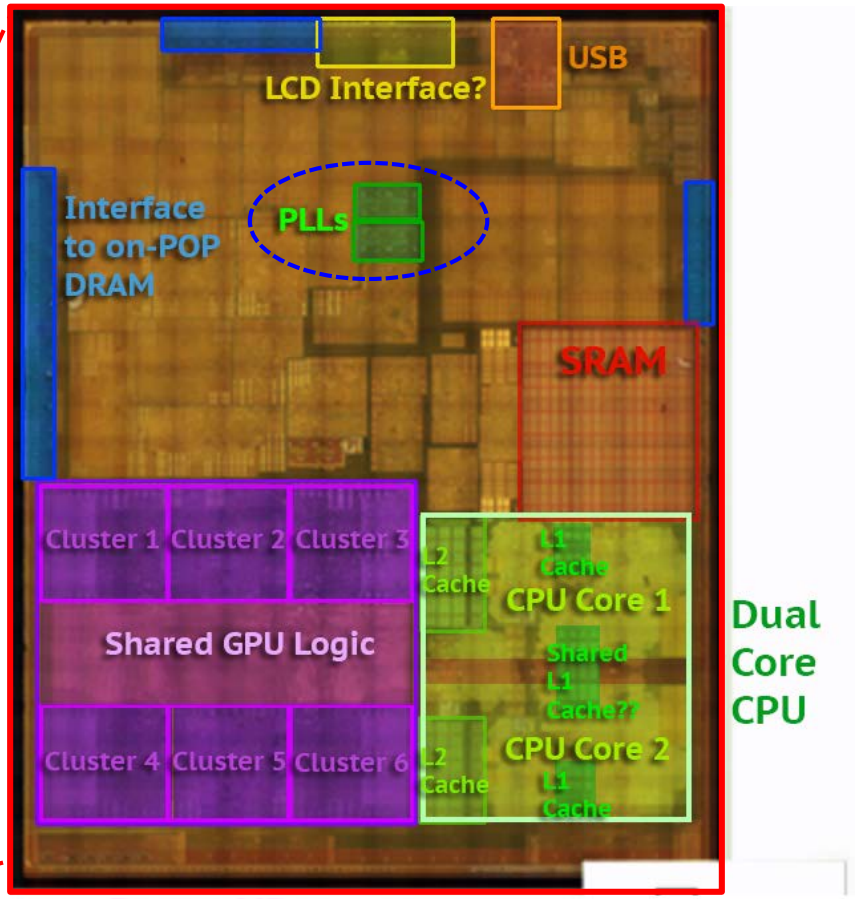
http://www.chipworks.com/en/technical-competitive-analysis/resources/blog/inside-the-a7/

How Are PLL's Used? (cont'd)

- iPhone 6



Operating frequency: 2GHz



Apple A8 Processor Floorplan

https://www.ifixit.com/Device/

http://www.dailytech.com/Die+Shots+Confirm+A8+Packs+Six+PowerVR+Rogue+GPU+Clusters/article36586.htm

How Are PLL's Used? (cont'd)

- **A8 vs. A7**

Apple A8 vs A7 SoCs		
	Apple A8 (2014)	Apple A7 (2013)
Manufacturing Process	TSMC 20nm HKMG	Samsung 28nm HKMG
Die Size	89mm^2	104mm^2
Transistor Count	~2B	"Over 1B"
CPU	2 x Apple Enhanced Cyclone ARMv8 64-bit cores	2 x Apple Cyclone ARMv8 64-bit cores
GPU	IMG PowerVR GX6450	IMG PowerVR G6430

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Design Considerations of PLL

- Output Phase Noise or Jitter (~dBc/Hz or P2P & RMS)
- Frequency Accuracy (~ppm or %)
- Frequency Range (e.g. 2.4GHz for GSM)

  ⇨ Adaptive Bandwidth Tracking

- Lock in Time (e.g. 280μs for GSM)
- Chip Area (~mm^2)
- Power Dissipation (~mW)

Design Considerations of PLL (cont'd)

- **Classifications of PLL Types**
  - **Analog PLL (APLL)**
  - **Digital PLL (DPLL)**
  - **All-Digital PLL (ADPLL)**
  - **Charge-Pump PLL (CPPLL)**

	CPPLL	DPLL	ADPLL
Approach	Mixed-signal	Mixed-signal	All-digital
Output Frequency	High	High	Low
Lock in Time	Slow	Slow	Fast
Area	Large	Large	Small
Jitter	Small	Small	Large

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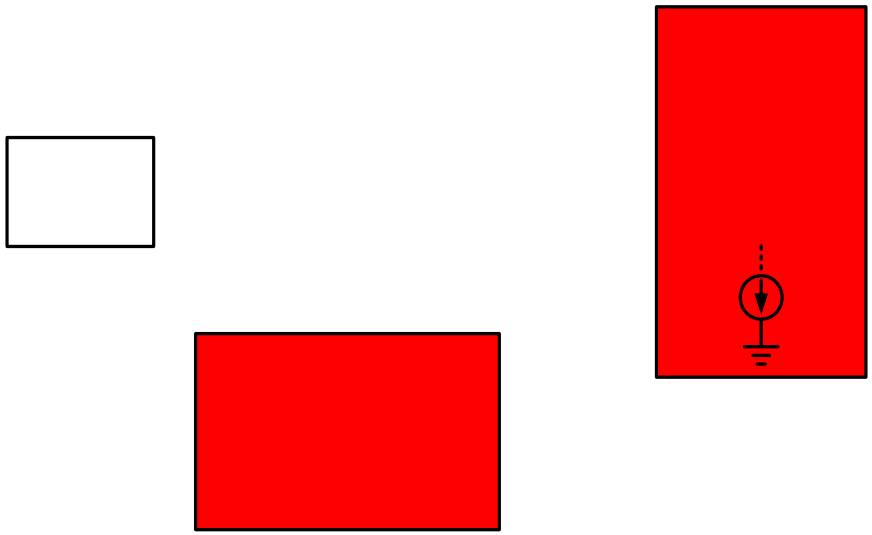
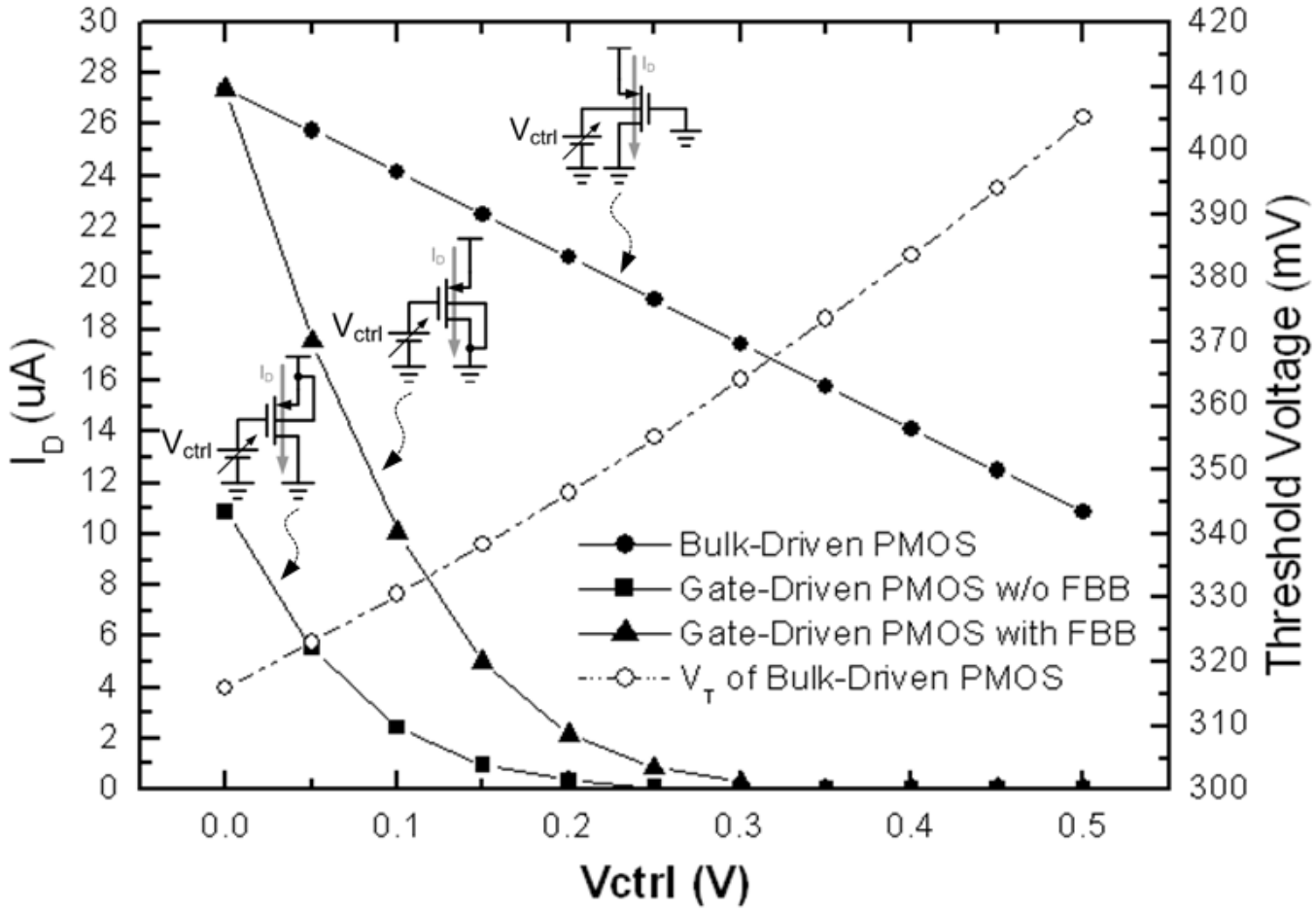
Proposed Low-Voltage PLL

- **Block Diagram of Proposed PLL**



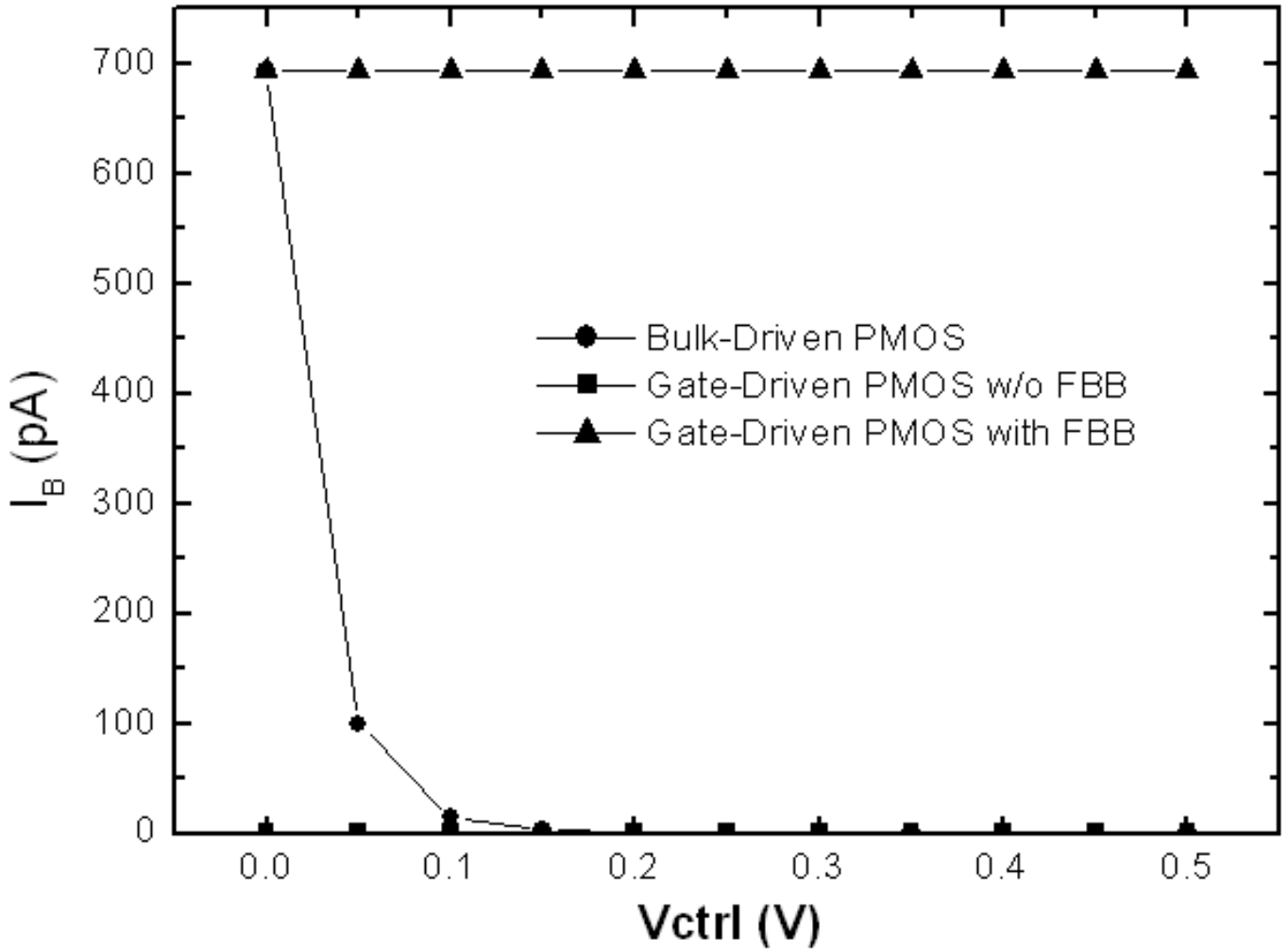
Proposed Low-Voltage PLL (cont'd)

- **Characteristics of Gate-Driven and Bulk-Driven PMOS**



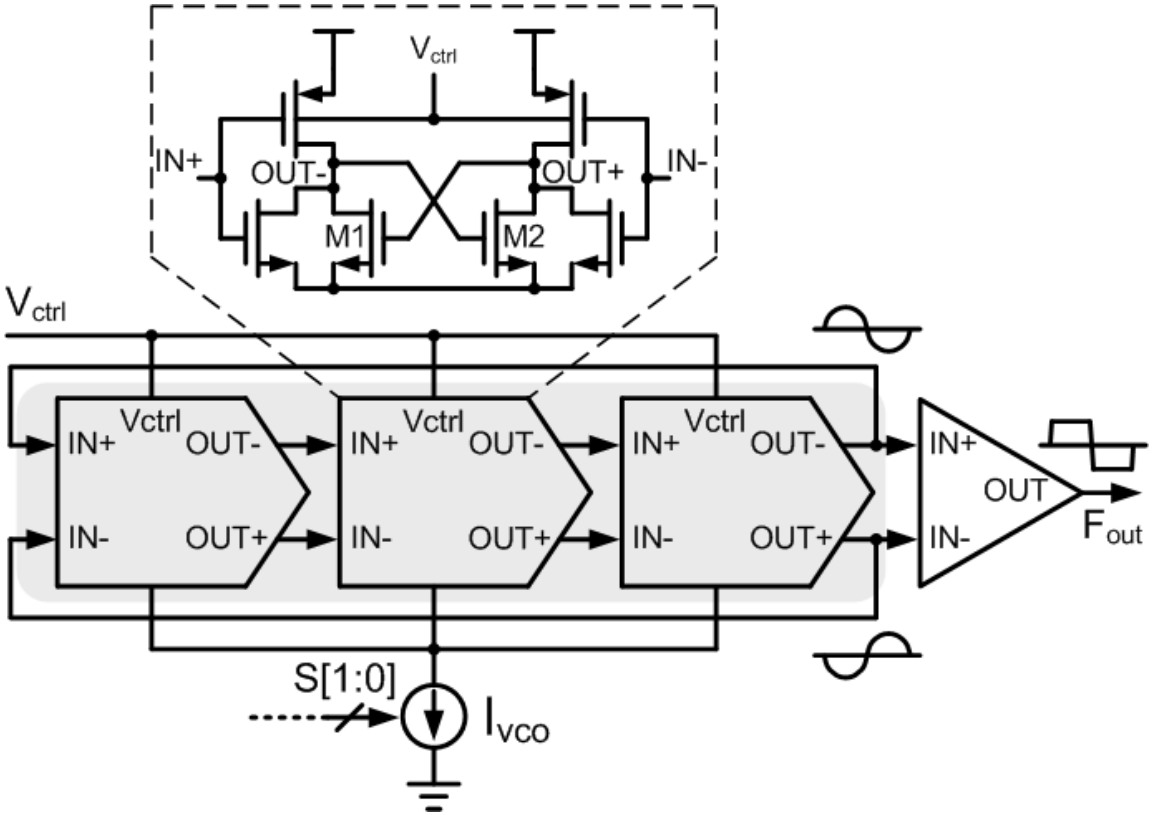
Proposed Low-Voltage PLL (cont'd)

- **Bulk Leakage Current of PMOS**



Proposed Low-Voltage PLL (cont'd)

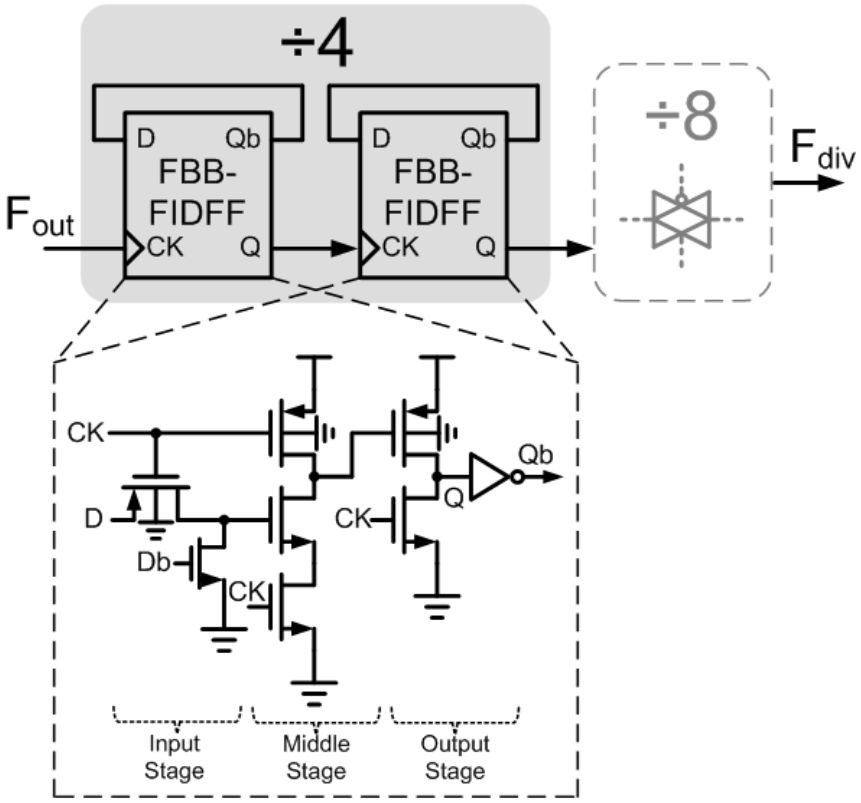
- **Bulk-Input VCO (BVCO)**



- **BVCO consists of a 3-stage fully differential ring oscillator and a differential-to-single-ended converter**
- **BVCO is digitally controlled using a 2-bit word (S1, S0) via the calibration circuit to avoid PVT variations**

Proposed Low-Voltage PLL (cont'd)

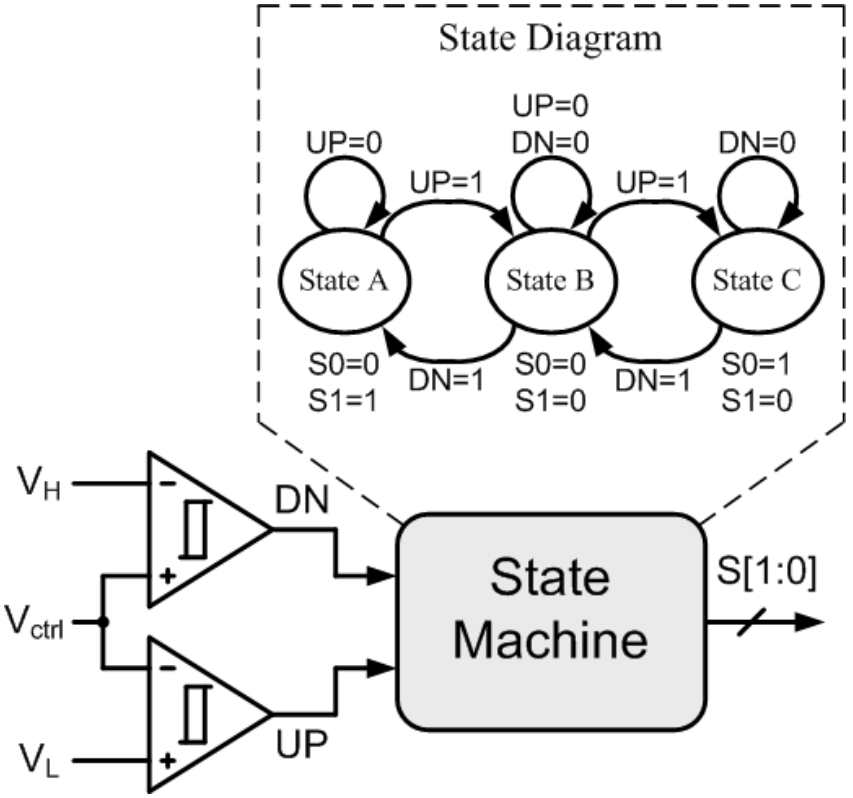
- **Divide-by-32 Counter**



- **The forward-body-bias and floating-input techniques are used in the proposed DFF (FBB-FIDFF)**
- **A divide-by-4 counter with the FBB-FIDFFs is the critical high-speed part, a divide-by-8 counter with the TGDFF in the second stage to reduce power**

Proposed Low-Voltage PLL (cont'd)

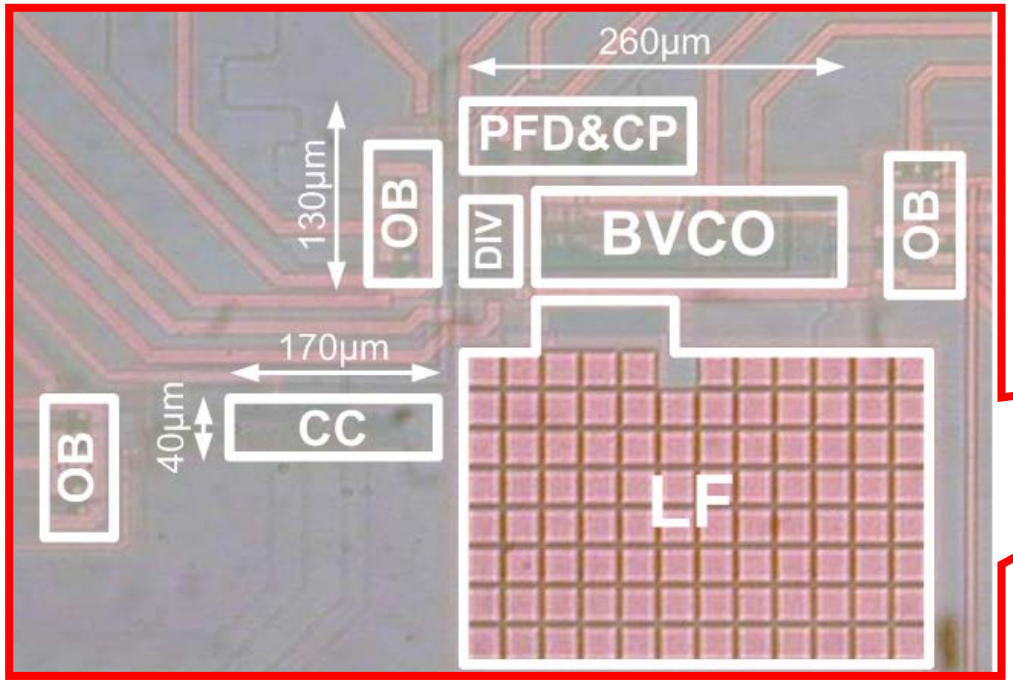
- **Calibration Circuit**

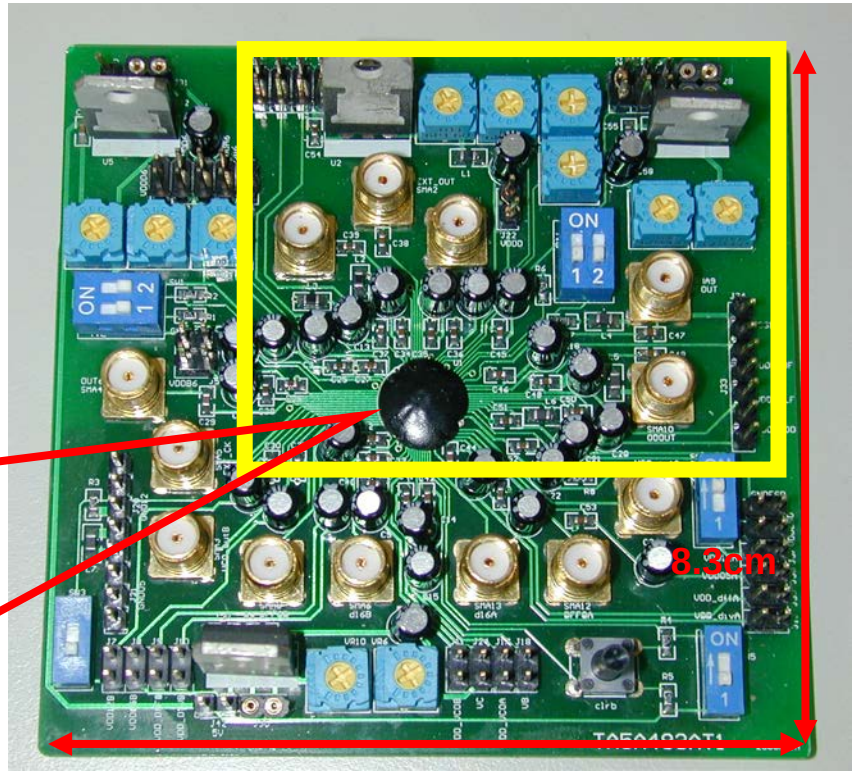


- **The calibration circuit consists of two comparators with hysterisis and the state machine circuit**
- **The 2-bit word (S1, S0) is according to the UP/DN signals to automatically adjust the current source of BVCO in various conditions**

Proposed Low-Voltage PLL (cont'd)

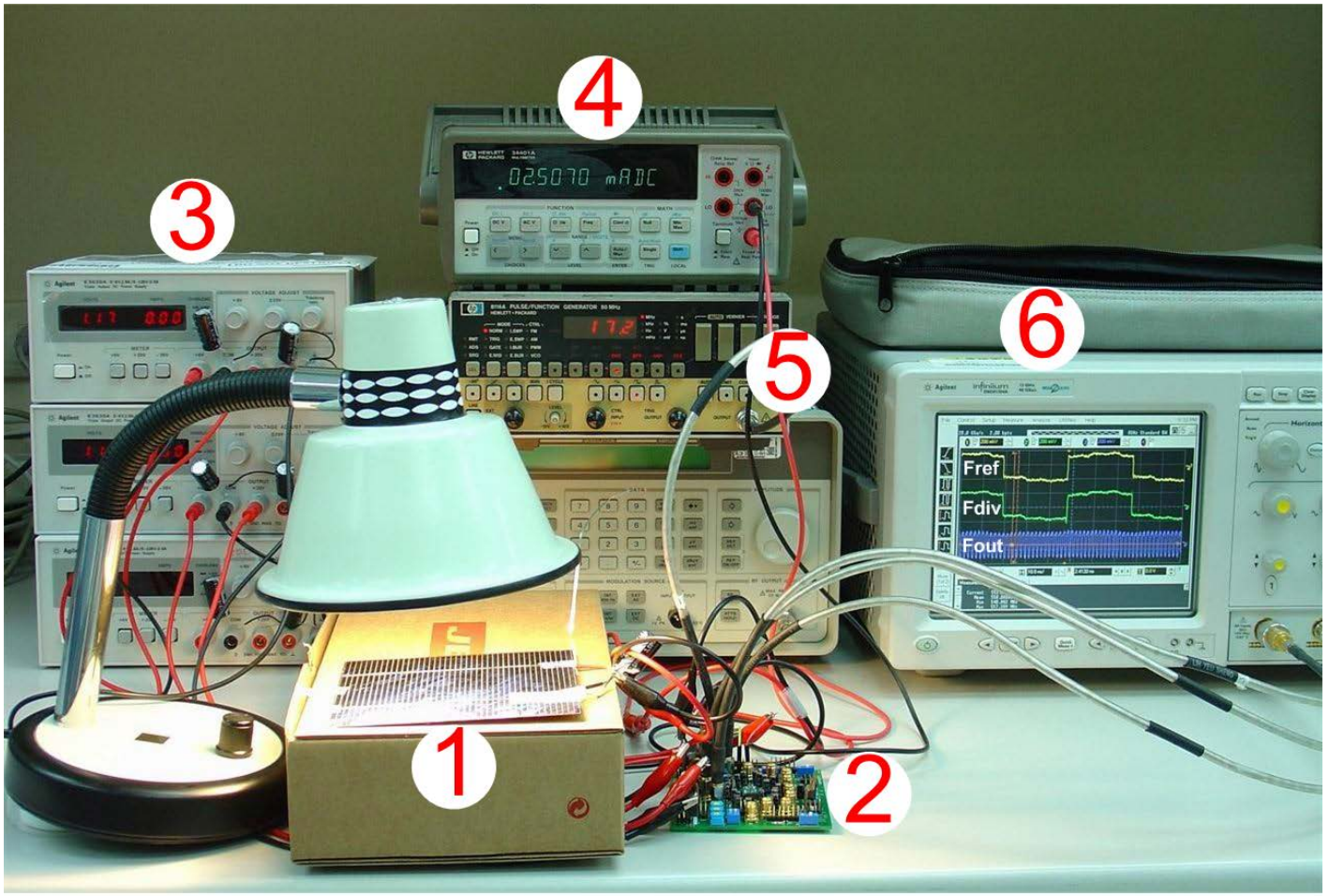
- **Microphotograph and Physical PCB**
  - The active area is 0.05mm^2





Proposed Low-Voltage PLL (cont'd)

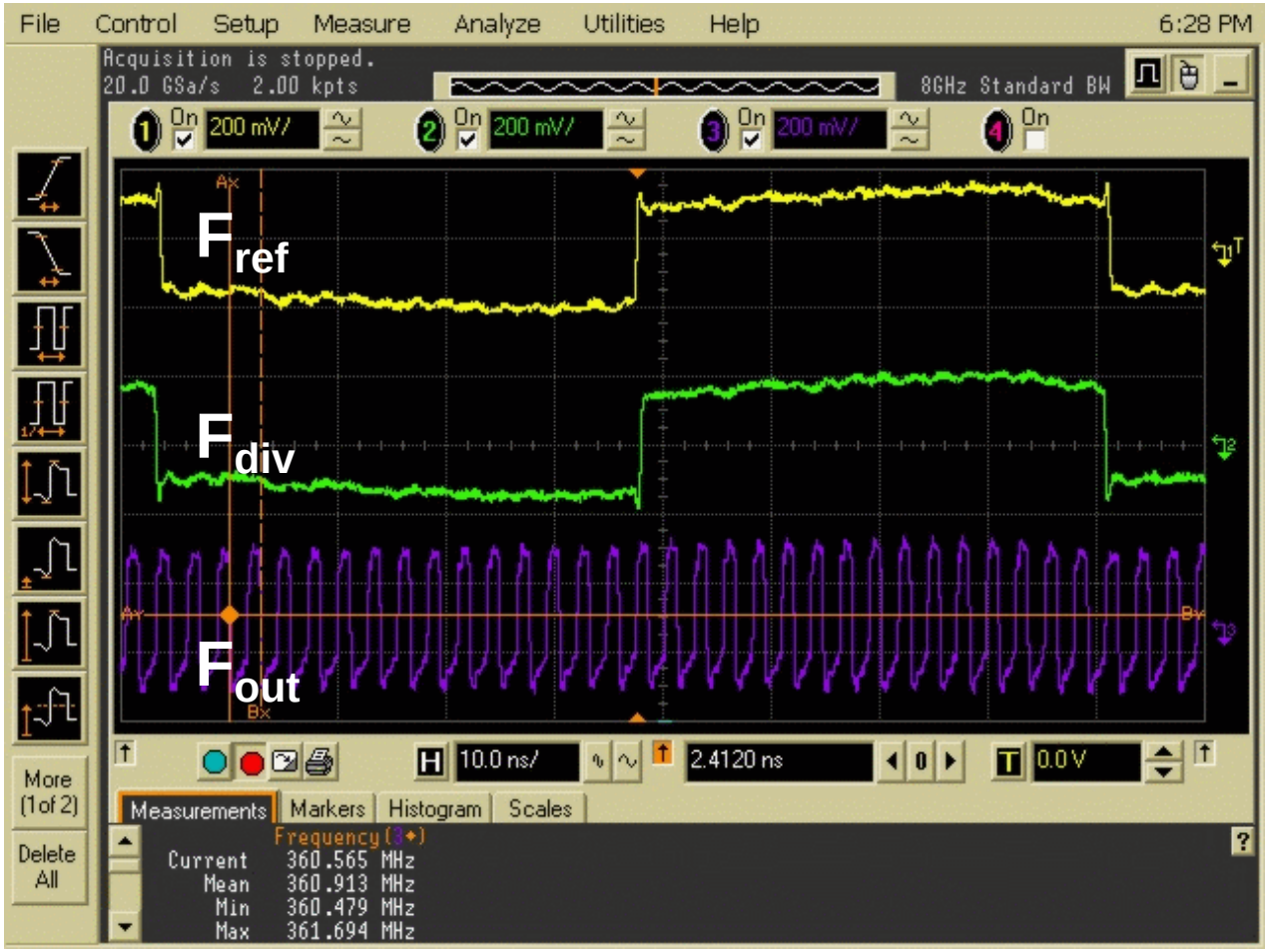
- **Measurement Environment**



1: Solar Cell
2: DUT
3: Power Supply
4: Current Meter
5: Pulse Generator
6: Oscilloscope

Proposed Low-Voltage PLL (cont'd)

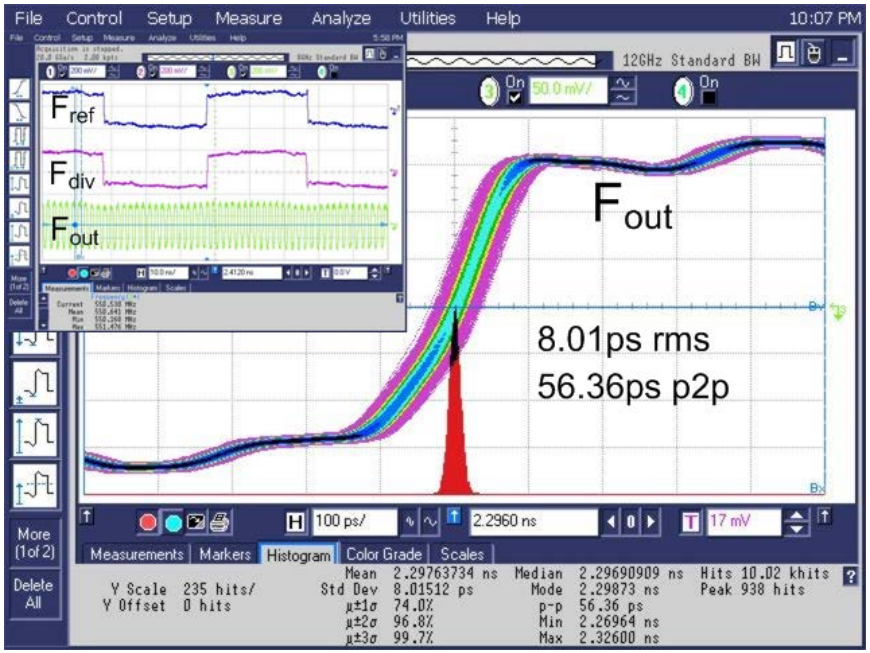
- **Measurement Results (1/3)**
  - **Measured Output Waveform (360MHz~610MHz)**



Proposed Low-Voltage PLL (cont'd)

- **Measurement Results (2/3)**
  - **Jitter Histogram at 550MHz**

- **0.5V Power Supply**



- **Single Solar Cell**

Proposed Low-Voltage PLL (cont'd)

- **Measurement Results (3/3)**

  - **Performance Summary**

Process	TSMC 0.13μm CMOS
Supply Voltage	0.5V (typical 1.2V)
Temperature	25^{o}
BVCO Tuning Range	306MHz~725MHz
PLL Frequency Range	360MHz~610MHz
RMS Jitter @ 550MHz	8.01ps (quiet supply) 8.76ps (solar cell)
Pk-Pk Jitter @ 550MHz	56.36ps (3.1%) (quiet supply) 67.27ps (3.7%) (solar cell)
Power Dissipation @ 550MHz	1.25mW
Lock Time	< 4.7μs
Active Die Area	0.05mm^2

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Conclusions

- An ultra-low-voltage PLL with bulk-input VCO is proposed.
- A VCO with bulk-input technique and a divider with forward-body-bias scheme to circumvent the V_T problem , enabling the PLL to be operated at an ultra-low voltage.
- The self-calibration technique is used to prevent PVT variations and maintain the desired operating frequency.
- The total power dissipation of the PLL is 1.25mW at an operating frequency of 550MHz with a 0.5V solar cell. The measured rms jitter and peak-to-peak jitter are 8.76ps and 67.27ps, respectively.

Thank you for your attention~